High-Voltage Signal Generator for Biomedical Applications

Jonathan M. Tse, B.E. (Hons)

A thesis submitted in partial fulfilment
of the requirements for the degree of
Master of Engineering
in
Electrical and Computer Engineering
at the
University of Canterbury,
Christchurch, New Zealand.

November 2011

ABSTRACT

Electroporation is the process where externally applied electric fields cause significantly increased permeability of the cell membrane. The increased permeability allows the transport of external compounds into the cell. This is important for applications in electrochemotheropy, electrofusion and drug delivery.

Electroporation also has applications in the disinfection of liquids. Given a high enough electric field across the cell membrane, the electroporation process can become irreversible, leading to cell destruction. With the cell membrane under an intense electric field, the cell membrane structure fails causing the cell to die. Conventional liquid beverage disinfection systems rely on slow heating methods requiring large power requirements; this can reduce the taste and quality of some liquids.

Pulse generators provide the necessary electric fields to produce the required voltage potential across the cell membrane. The usefulness of electroporation depends on several parameters such as amplitude, frequency and rise/fall times of the electric field. The wave shape also has a bearing on performance, and is limited by the pulse generator topology. A multilevel bipolar waveform is desired with operating frequencies above about 1 kHz. The cascaded H-bridge or full-bridge topology is the most useful as it capable of producing multilevel bipolar waveforms at high frequency.

This thesis presents the design and implementation of a multilevel high-voltage pulse generator, capable of creating very high-voltage AC pulses. MOSFET switching devices in conjunction with good layout practices were used to provide required fast switching speeds. The full-bridge topology is used to create a multilevel output profile through cascading of multiple stages. As a full-bridge topology inherently creates a RCL resonant network, there are many challenges associated with mitigating high-frequency noise sources.

Two separate stages are built, a low voltage stage capable of outputting up to 200 V_p and a high voltage stage capable of switching up to 1 kV_p. A control board was also built for pulse signal generation and user configuration of the output waveforms. The designed pulse generator can produce short pulses of up to 1.4 kV_p at frequencies of up to 350 kHz using primarily resistive loads (that simulate a conductive liquid load). Little high frequency switching noise was observable on the output waveform.

A single stage pulse generator was also tested with actual liquid loads using an

electrode chamber, demonstrating electroporation. The liquid load testing was performed on water and milk derived from milk powder. Results showed that the liquid loads were consistent with primarily resistive loads.

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my supervisor Dr. Paul Gaynor for his time and effort into helping me undertake this project. I thank him for his patience and guidance through the project. I would like to thank the ECE workshop technicians Nick Smith and Ken Smart who helped me with building PCBs and setting up the testing equipment. Thanks to Tom Cronje whose experience, knowledge and assistance was invaluable throughout the project. Thanks also go to Jonathan Bousfield who helped me with the project in the later stages. Lastly thanks go to my parents for their support and encouragement throughout my studies at the University of Canterbury.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

NOTATION

CMRR	Common-mode rejection ratio
DC	Direct Current
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input and Output
HV	High Voltage
IC	Integrated Circuit
LV	Low Voltage
MCU	Micro-controller Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PSU	Power Supply Unit
TTL	Transistor-transistor logic

NOMENCLATURE

Symbol	Definition	Unit
$\mathbf{C_{iss}}$	MOSFET input capacitance	F
$\mathbf{C_{oss}}$	MOSFET output capacitance	F
$\mathbf{C_{rss}}$	MOSFET reverse transfer capacitance	F
$\mathbf{C_{gd}}$	Gate to drain capacitance	F
$\mathbf{C_{gs}}$	Gate to source capacitance	F
$\mathbf{C_{gs}}$	Gate to source capacitance	F
$\mathbf{C_{th}}$	Gate to source threshold voltage	F
$\mathbf{C_{bs}}$	Bootstrap capacitance	F
$\mathbf{I_{LKCAP}}$	Capacitor leakage current	A
$\mathbf{I_{LKGS}}$	MOSFET gate leakage current	A
$\mathbf{I_{LK}}$	Bootstrap leakage current	A
$\mathbf{I_{LKDIODE}}$	Bootstrap diode leakage current	A
$\mathbf{I_{QBS}}$	Quiescent current of bootstrap circuit	A
$\mathbf{R_g}$	Gate resistance	Ω
$\mathbf{R_{ds}}$	Drain-source ON resistance	Ω
$\mathbf{V_{pp}}$	Peak to peak voltage	V
$\mathbf{V_{gs}}$	Gate to source voltage	V
$\mathbf{V_{ds}}$	Drain to source voltage	V
$\mathbf{Q_{total}}$	Total bootstrap charge	C
$\mathbf{Q_{gate}}$	Gate charge	C

Chapter 1

INTRODUCTION

This chapter introduces the motivation of building a high-voltage signal generator and the practical applications in the electroporation field. The reasoning for using high magnitude bipolar electric fields on biological cells is explained and the use of power electronics to achieve this. A belief review of existing liquid disinfection studies through high voltage pulses is given. Commercially available high voltage devices are also outlined including the inadequacies of these devices. An outline summary of the thesis is also given.

1.1 MOTIVATION

The quality of drinking water is a factor that is taken for granted. Enteropathogenic microorganisms such as cholera and salmonella can cause gastrointestinal infections. In third-world countries this is more prevalent as there is in many cases of inadequate sanitation practices associated with much larger population densities. New Zealand generally has excellent water quality that is filtered naturally; however, pathogens such as *Giardia intestinalis, Cryptosporidium parvuum* and *Campylobacter jejuni* still appear in some of New Zealand's water supplies. Water quality is dependent on water delivery from the original source to the eventual user of the water. Biological and inorganic compounds could be introduced to water supply at any stage from treatment to transportation. This has created a market for portable or installable water treatment systems in homes. There are various common treatment methods, such as particle or carbon filtration, ultraviolet light, and distillation. Additionally, the use of high-magnitude electric fields has been demonstrated to dramatically reduce both biological and inorganic compounds within water [Johnstone 2001].

Ordinary liquid consumables, such as milk and juice, can also contain harmful bacteria, even though treated during production. The standard method for liquid disinfection consists of heating to kill microorganisms (pasteurization). However, pasteurization can cause undesirable effects such as discoloration and reduced taste [Wetz et al 2004]. An example of a non-heating method is ultra-violet (UV) light. This has

low penetration capability, therefore, is only suitable for surface sterilization [Rao 2008]. The use of electric fields for disinfection is seen to be a non-thermal method with low energy requirements [Castro et al 1993]. The quality of the liquid is not reduced with little change in the nutritional content [Oka et al 2009].

The secondary aspect of this research is to a obtain better understanding of electroporation mechanisms. There has been some research into electroporation that identifies the need for a high frequency and high-voltage bipolar pulse generator apparatus. This will give researchers the ability to investigate a new understanding of electroporation for liquid disinfection purposes.

1.2 ELECTROPORATION MECHANISMS

Electroporation is the effect of inducing electric fields across biological membranes so they exhibit enhanced permeabilization effects; the cellular membrane experiences molecular rearrangement in the form of nanoscopic pores [Rubinsky 2007]. When a transmembrane electric potential is created, large enough to induce electroporation, this results in either reversible or irreversible membrane permeabilization [Johnstone 2001]. A reversible permeable membrane allows transient transmembrane transport of macromolecules in and out of the cell which leaves the cell in a viable state. This has vast applications such as electrochemotherapy, electofusion of cells, drug delivery for cancer cells, water disinfection and food preservation [Teissie et al 2002]. Irreversible permeabilization of biological cells usually destroy the cell, and thus is applicable to water purification and other food disinfection applications where biological cells need to be destroyed.

1.2.1 Cellular Mechanism

A biological cell has several mechanisms for allowing molecules into and out of itself in order to survive. The cell consists of a lipid bilayer membrane which is a semipermeable structure that limits movement of molecules in and out of the cell. The type of material being able to pass through is dependent on the biochemical structure of the membrane. Small molecules such as water can pass through the membrane, whereas molecules such as glucose are restricted as they are larger. In order for the cell to maintain survival, the cell membrane needs to maintain functionality or cell death may occur [Atlas 1988].

A cell can be classified as *prokaryotic* or *eukaryotic*. Prokaryotic cells include all bacteria. These cells consists of a simple structure that do not contain *organelles* like that of eukaryotic cells. The organelles within the eukaryotic cell have specific functions such as storage or energy production. The makeup of the prokaryotic cell is more complex and is associated with multi-cellular lifeforms such as plants, animals and

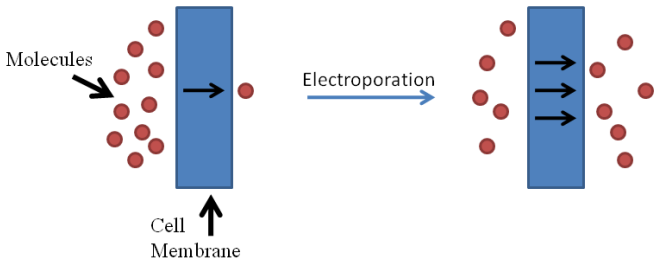


Figure 1.1 Defusion of molecules through a cytoplasmic membrane caused by a significantly increase transient permeability.

fungi. Both fundamental types of cells transport material into and out of themselves through their membrane wall in order to function and survive.

1.2.2 Electrical Model of a Cell

The electrical properties of a simple cell structure can be modeled as a network of parallel connected resistors and capacitors. The cell membrane has a higher resistance and capacitance compared to inside and outside the cell membrane. A simple resistive and capacitive network is shown in Figure 1.2 for basic illustrative purposes. A cell membrane typically has a capacitance of 1 μF/cm^2, while inside the cell the resistivity is around 100 Ωcm [Schoenbach et al 1997].

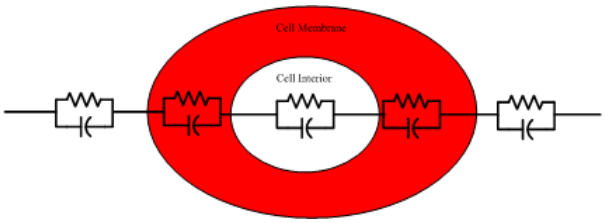


Figure 1.2 Resistive and capacitive electrical network model of biological cell.

The cell can also be modeled in a suspension medium as a spherical particle with a form factor $f = 1.5$. The cell is modeled in a suspension medium with two parallel plates producing an electric field. There is a critical transmembrane voltage value V_c whereby the cell starts to exhibit enhanced permeabilization effects and is approximately 0.2-1.0 V for a wide range of biological cells [Rae and Levis 2002]. The critical voltage value is given by the formula

$$V_{MI} = 1.5 E_o a \cos(\alpha) \pm V_m \tag{1.1}$$

where, α is the angle between the field direction and membrane site, E_o is the critical external electric field applied, a is the cell diameter and V_{MI} is the resting transmembrane potential. Due to the subtracting effect of electric fields, cell perme-

abilization becomes more apparent near the positive electrode, this is illustrated in Figure 1.3 [Johnstone 2001].

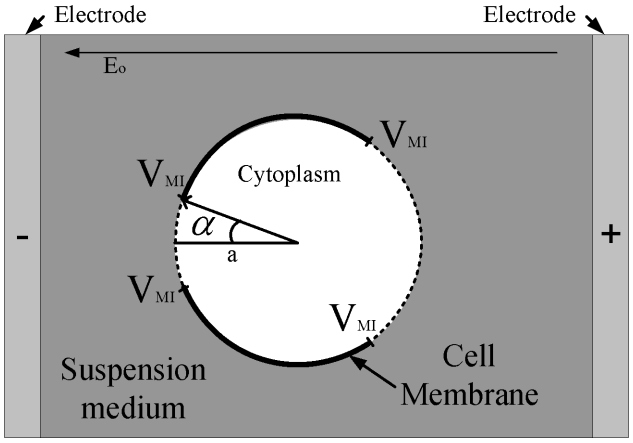


Figure 1.3 Spherical model of biological cell in a suspension medium

1.3 PREVIOUS STUDIES AND APPLICATIONS

Electroporation is used for gene transfer and chemotherapy [Pavselj and Miklavcic 2008]. In these applications, electroporation is usually produced by inducing a DC capacitive pulse discharge across biological cells of interest. Transient permeability of cells can occur if a transmembrane potential is achieved from an applied electric field. The cells rate of macro-molecule intake can therefore be greatly increased.

While most electroporation applications only cause transient permeability, total destruction of the cell may be desirable. Applications such as water disinfection and food conservation, are two such areas where total cell death is desirable. When an intense electric field , much greater than the critical electric field value required for electroporation, is applied, cellular lysis may occur. Cellular lysis is a state whereby the cell membrane has been irreversibly compromised and allows the cell interior to reach chemical equilibrium with its surrounding media. During electroporation, larger cells are more effected from externally applied electric fields as the transmembrane potential for these cells is higher due to their larger radii (equation 1.1). This means that for smaller cells, higher electric fields need to be applied to achieve the required V_{MI}. As it is seen that enhanced membrane permeability occurs when a transmembrane potential between 0.2-1 V is induced, this requires an applied external electric field in the order of 1 kV/cm. As electrodes used for electric field generation are usually separated by more than a few mm, the applied voltages required are in the order of 10^2 - 10^3 V.

1.3.1 Water Disinfection through Electroporation

There has been considerable research done into producing a water disinfection system using high electric fields. Paul Johnstons PhD project at the University of Canterbury used high voltage bipolar pulses at frequencies lower than 1 kHz to induce electroporation effects. A 99.9% destruction rate for *Giardia* was found when using a 50 Hz high voltage treatment. A higher frequency system was implemented using a 3 kV_p, 17 kHz system which considerably reduced the energy requirements compared to the 50 Hz system. The idea is that higher frequencies leads to reduced power requirements as the exposure time for electric fields can be reduced while still yielding acceptable destruction rates. The rate of destruction of bacteria was also found to be dependent on the metabolising state of the cells. This meant that some cells are less susceptible to high electric fields when in a non-metabolising state. When in water, bacteria are mostly in a non-metabolising state which can make high cell destruction rates harder to achieve. Destruction rates of 99% were shown in initial testing. With increased flow rates, destruction rates were reduced. Higher frequencies were also shown to reduce electrolysis effects that cause electrode degradation.

The electrode arrangement has as effect on performance in terms of usable flow rate and effectiveness at disinfection. The effects of electroporation can be maximized by using minimal distance in order to increase electric field strength; however, this can decrease flow rate. A cylinder arrangement was designed by Paul Johnston in order to maximize electric field strength ideal for electroporation conditions. In order for reliable operation, trapped air is removed from the water before it flows past the electrodes. Bubbles in the water can cause electrode arcing as the electric field nonlinearity caused by the air bubble can lead to ionization of the water (dielectric breakdown). If air bubbles are not mitigated, electrode arching is more likely to occur before useful electroporation of the cells and could lead to failure of components.

1.3.2 Disinfection of Beverages

There have been a number of other studies into disinfection of consumable liquids. In one paper it was found that using a field strength of 43.4 kV/cm caused a log 6.3 reduction in the inactivation rate of *E. coli* in simulated milk [Alkhafaji and Farid 2007]. This paper details use of a full bridge topology using insulated gated bipolar transistors (IGBT) to produce bipolar pulses. The pulse generator system was design with a high-voltage transformer raising the 1 kV output from the full-bridge to a 30 kV output. Very short pulses were used so to limit the thermal effects on the treated media. Pulse rise times were of around 0.5 μs due to IGBT limitations. It was found that higher electric field strength had a major bearing on destruction rates.

Another study has also shown that high-voltage AC waveforms are more effective at liquid food disinfection as shown in [Hanifah et al 2010]. It was seen that exponential

decay type pulses and oscillatory type pulses had reduced effect on sterilization. In this study a cascaded H-bridge design was proposed to produce bipolar pulses of around 6 kV through low frequencies below 100 Hz but with pulse widths of around 1 μs.

Further research has been conducted to identify parameters of liquid in terms of a resistive parameter [Jayaram et al 2005]. A capacitive discharge topology was used to produce a damped sinusoidal output waveform. The pulse shape is found to be influenced by the electrode arrangement, type of treated liquid and pulse generator components. Using a parallel electrode arrangement with a 50 mm diameter, resistances of 5.85 Ω, 8.00 Ω, 1.25 Ω were identified for orange juice, apple juice and tomato juice respectively. Increased inductance through electrode arrangement or ground loop caused significant increase in oscillations. Control of the pulse shape is harder to achieve through a capacitive discharge pulse generator.

1.4 EXISTING ELECTOPORATION DEVICES

There are readily available electroporation devices in the marketplace. BTX make pulse generator devices suitable for cell transfections and bacterial electroporation [BTX 2011]. These are more suited towards research areas applicable to electrofusion, and bacteria and yeast electroporation, where power requirement is low. The ECM 830 Electroporation system from BTX has low and high voltage settings. The low voltage setting capable of 10 μs pulses at 500V while the high voltage setting is capable up to 3000 V with a pulse width of 1 us. This is a DC single pulse system which uses a capacitive discharge type of topology. However, pulsed AC electric fields have been shown to be more efficient at electroporation [Chen et al 2008].

A study of electroporation devices has been conducted in Puc et al [2004]. In this paper typical techniques for generating high-voltage is explored including capacitor discharge, square waves using transistors, pulse transformers and modular high-voltage sources. The use of square waves using semiconductor switches is useful as it is simple to design and the pulse output parameters can be easily controlled. It details a variety of commercial devices being compared with voltage capability, frequency limitations and charging times. However, it is difficult to make comparisons as each device has specific limitations dependent on the application. It is seen that the characterization of the load is difficult to determine. Heating of the treated material as well as electrode contamination are undesirable effects of high voltage pulses with long exposure times. Currently, most devices are suited towards research applications as electroporation is actively being researched.

1.5 RESEARCH OBJECTIVE

A DC-AC pulse generator is to be designed and constructed. Using modern DC power supplies, a suitable topology should be chosen to produce bipolar AC waveforms specific to liquid disinfection and electroporation research with specifications listed in Table 1.1. As such, the system is to be user configurable. Switching speeds should be optimized through careful consideration to components and good layout technique. Fast rise and fall times output pulses are desirable for high electric field strength leading to better electroporation efficiency. 1 kV pulses of around 200 kHz should be considered for water purification. The system is to be user configurable as electroporation is still open to research which may call for various pulse shape specifications. Multiple voltage stages should also be considered. Figures 1.4 and 1.5 show the desirable waveform shapes for a five level output.

Table 1.1 High Voltage Signal Generator pulse specifications

Parameter	**Value**
H-Bridge Stages	2
Maximum Voltage	2000 V_{pp}
Maximum Frequency	200 kHz
Switching current	> 1 A
Low Voltage Output Stage	400 V_p
Low Voltage Output Pulse width	50-500 μs
High Voltage Output Stage	1000 V_p
High Voltage Output Pulse width	1-20 μs

1 kV_p pulsed AC waveforms are required to achieve adequate transmembrane permeabilization of cells. Higher voltages may be required if electrode separation is increased. The system is to be designed for high frequencies for power efficiency while maintaining suitable destruction rates of cells. Liquid disinfection through electroporation is still actively being researched, therefore the system is to be configurable. Two voltage levels are used in order to research the ability to reduce system power while maintaining disinfection levels. The device should be suitable for high current pulsed applications. The load impedance relates to the resistive and capacitive nature of the liquid being treated. These are variables which are dependent on liquid properties, electrode arrangement, voltage and type of waveform.

1.6 SUMMARY

Producing AC waveforms using full-bridge topology circuits is becoming more popular as it is simple to design and allows multilevel cascading [Corzine and Familiant 2002].

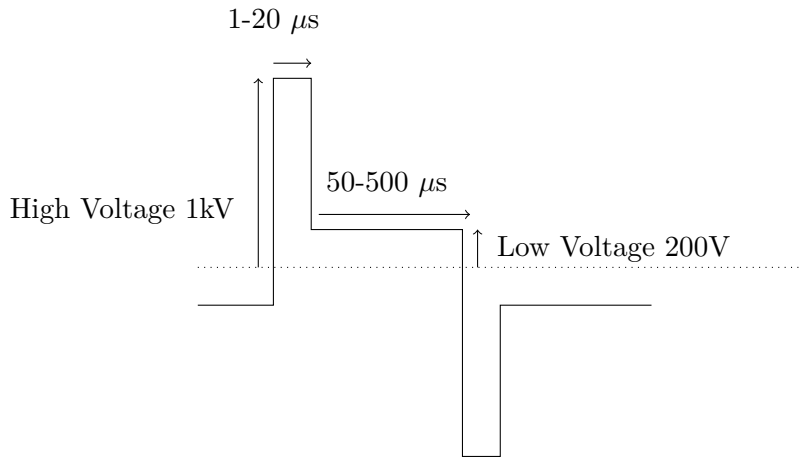


Figure 1.4 Single cycle of an AC waveform expected for liquid disinfection through electroporation

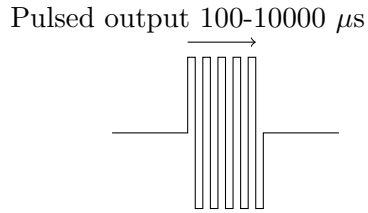


Figure 1.5 Pulse waveforms for electroporation made up of multiple AC waveform cycles

This requires the use of high voltage semi-conductor switches (mainly MOSFETs) and adequate driving signals to produce waveforms with minimal distortion. Various designs have been produced for electroporation applications. Advances in power MOSFETs mean they have higher current ratings and therefore higher power. Driving MOSFETs as fast as possible at high frequencies has become a challenge for engineers and thus the need for dedicated MOSFET driver ICs. Some MOSFETs are rated for voltages in excess of 1000 V. The potential for catastrophic failure of such high voltage and high power devices is a serious issue.

The project involves the design and construction of a pulse generator using modern power electronic design concepts. The system is to be user configurable as many aspects to electroporation research remain unknown. With the ability to specify a waveform shape, this gives researchers a greater understanding to electroporation dynamics. As the system is for research purposes, it is ideal that it can be easily adapted for the specific electroporation application. The use of fewer power supplies, while designing the system to be in a compact form, is desirable.

The system is to be tested with realistic loads expected for high power electroporation applications. The system is also to be tested on actual liquids to assess the viability for disinfection applications.

1.7 THESIS OUTLINE

This thesis consists of six chapters excluding associated appendices. **Chapter 2** introduces basic DC-AC topologies appropriate for the generation of bi-polar pulses in the application of electroporation. The function of the full-bridge topology in multilevel designs is detailed. Cascaded topologies is also discussed and the type of hardware required. The signaling required for a cascaded configuration is shown.

Chapter 3 covers the characteristics of power MOSFET devices, level-shift techniques, isolation, and gate drivers. The power MOSFET switching characteristics, which can affect pulse generation performance, are detailed.

Chapter 4 presents the design of the high-voltage signal generator and the hardware implementation. The H-bridge signaling for multi-level applications produced from digital hardware is shown. PCB layout issues that cause noise are addressed as well as the power supply requirements.

Chapter 5 provides the results observed during pulse generator operation with the testing procedures undertaken. Primarily resistive loads are tested including simulated liquid loads for disinfection applications.

Chapter 6 concludes the Masters thesis outlining major goals achieved and possible improvements for future research.

Chapter 2

SIGNAL GENERATOR AND SWITCHING DEVICES

The specifications for the high voltage pulse generator have been outlined in Chapter 1, as well as background to electroporation mechanisms for cellular destruction. Previous research studies in the areas of electroporation have been briefly explored.

This chapter lists various topologies, useful for high voltage switching. Limitations of switching devices are explained and how it can limit a pulse-generator's performance. The basic H-bridge design is explained in detail, and how a multilevel output profile can be achieved.

2.1 SWITCHING DEVICES

In this section various semiconductor switching devices are explored that historically have been used for the SMPS(Switch Mode Power Supply) industry [Randall 2005]. Bipolar junction transistors (BJTs), metal oxide silicon field effect transistors (MOSFETs), insulated gated bipolar transistors (IGBTs) and thyristors are considered for pulse generator applications. Figure 2.1 illustrates capabilities of common semiconductor power electronic switches [Mohan et al 2003].

Ideally a switch turns on and off instantaneously in order for reliable operation at high frequency. However, practical switches are not ideal, blocking voltage capability vary in each device. While high di/dt is desirable, di/dt exceeding switch specifications may cause concentrated areas of current flow which can damage the component. Excessive dv/dt may cause excessive current flow through the switch junction. Gate control requirements add to overall power consumption and are important for assessing power losses [Rashid 2003]. Device characteristics need to be considered in all switching devices for use in a pulse generator design.

2.1.1 Bipolar Junction Transistor

Bipolar Junction Transistors (BJTs) are current controlled devices and consist of NPN and PNP type junctions. A forward biased pn junction in a BJT consists of a parallel depletion and diffusion layer capacitance. Compounded with the Miller effect, the

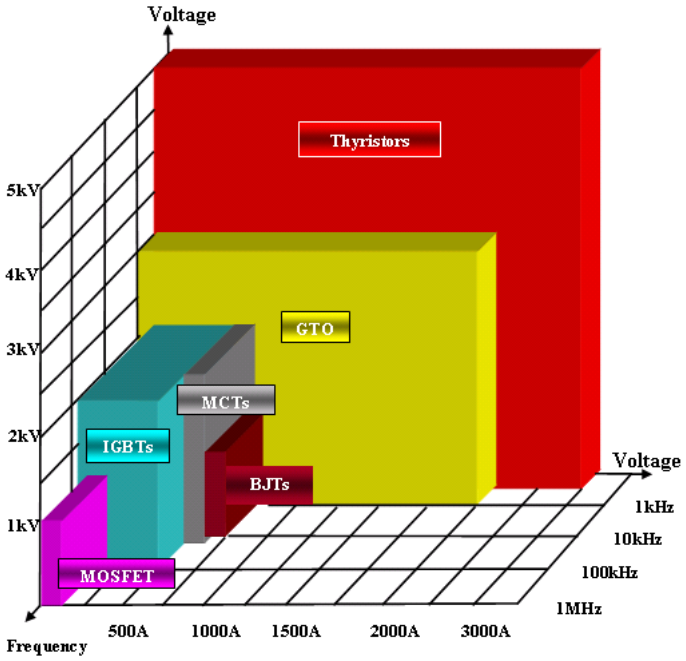


Figure 2.1 Diagram of common Semiconductor Switching Devices with voltage, frequency and current capabilities [Mohan et al 2003]

input capacitance is significantly large. BJTs exhibit low on-state resistances; however, the control of the device requires high base current. BJTs also suffer from a second breakdown voltage whereby the collector-emitter voltage drops significantly which leads to large power dissipation and excessive heating in a localized region of the device. This failure mode is the result of thermal runaway and ultimately leads device destruction. BJTs are considered for applications rarely exceeding frequencies in the range of 10 kHz. As charge recovery time and switching speed is slow there are high switching losses. [Rashid 2003].

2.1.2 Metal-Oxide Silicon Field Effect Transistors

Power MOSFETs are voltage controlled devices which require less power for switching control making them ideal for fast switching and low switching losses. The gate is isolated from the conducting materials; therefore, the ON state does not require a constant current. Commonly used in higher frequency applications of up to around 1 MHz, they are suitable for switching rise and fall times of around a few nano seconds. The maximum current capability of low voltage MOSFET devices are in the order of hundreds of amps and they are typically used in relatively low power applications. Modern high-voltage MOSFET devices have breakdown voltages rated to around 1 kV [Rashid 2003]. Microsemi for example, produce MOSFETs with breakdown voltages of up to 1200 V with drain currents in the order of tens of amps [Microsemi Corporation 2011]. MOSFETs are positive temperature coefficient devices, in which as the

temperature of the device increases so too does the internal resistance, reducing current capability [Ball 2005]. Generally, power MOSFETs exhibit low ON state resistances, fast switching speeds and low power gating requirements that is not associated with other devices [Barkhordarian 2005]. Electrostatic discharge and short-circuit problems are associated with MOSFETs [Rashid 2003]. MOSFETs exhibit lower power requirements than BJTs and have a wider safe operating area [Oh 2000].

2.1.3 Insulated Gated Bi-polar Transistor

Insulated Gated Bipolar transistors (IGBTs) are considered for higher power switching; however, are suitable for applications where the frequency is less than around 100 kHz. They are considered as providing a compromise of benefits from both MOSFETs and BJTs. Like the MOSFET, the IGBT is a voltage controlled device, although the physical structure is similar to that of the BJT. The advantages of IGBTs are higher voltage blocking capabilities of up to around 4 kV. Current handling capability however far exceeds that of MOSFETs, in the order to kilo-amps, suitable for higher power applications. It is known that IGBTs exhibit low on-state resistances due to conductivity modulation. IGBT, are also easier to control. However, they can exhibit latch-up behavior whereby the device is forced into conduction if a critical pulsed current value is exceeded [Sattar 1998].

2.1.4 Thyristors

Thyristors conduct current in one direction, from anode to cathode through a low impedance path. A gate current is used to turn the device on. Once in a conducting state the device is latched on. Thyristors have many uses in power electronic applications such as capacitor discharge ignitors, motor control and power supplies. As the thrystor can not be turned off via gate, external circuitry is required to turn the device off. The anode is required to be negatively biased to turn the device off. They are generally known as being robust devices [ON Semiconductor 2006], however, switching times are large due to control mechanisms. Current and voltage capability of thyristors still exceed that of modern BJTs and MOSFETs. They are used for switching applications up to around 500 Hz, with voltage and current capabilities around 5 kV and 3 kA respectively [Mohan et al 2003].

2.2 SIGNAL GENERATOR TOPOLOGIES

There are various pulse generator topologies that are effective for electroporation applications. Capacitive discharge, resonant converters, boost array converters and full-bridge inverters have seen applications in pulse generation. It is seen that one of the problems with designing a pulse generator are the unknown characteristics of the load

[Puc et al 2004]. The resistive and capacitive components of the load depend upon geometry and material of the electrodes as well as the electrical and chemical properties of the treated sample. Parameters such as voltage, frequency and period have a bearing on the overall efficiency of the application. These parameters are modified by selecting the appropriate topology for the application.

2.2.1 Capacitive storage Discharge

Capacitive discharge devices are the most simplest pulse generators used in electroporation. The output waveform is an exponential decay pulse delivered to a predominantly resistive load. The topology consists of a power supply, switch and an optional resistor to set the discharge time constant. To maintain pulsed output, the capacitor energy should be one or two times greater in magnitude than the energy of the pulse [Teissie et al 2002]. As shown in Figure 2.2 this illustrates a basic capacitive discharge circuit. The charging state charges the capacitor through a current limiting resistor R_{ch} to limit high peak currents from the power supply. The capacitor voltage is able to rise to the power supply voltage. During the discharging state, the charge stored in the capacitor discharges through the parallel resistor and load impedance $R\|Z$. The rate of discharge is dependent on the parallel resistor and load impedance, and the capacitance C_s. The rate of discharge is given as $V_{cap} = V_o e^{-t/(R\|Z)C_s}$, where V_{cap} is the capacitor voltage, and V_o is the initial charge voltage of the capacitor. This topology is simple to design. However, due to large charging times of the capacitor and variable load conditions; it is not suitable for repetitive pulsing. Sparking can also occur in the switch requiring additional circuitry [Puc et al 2004].

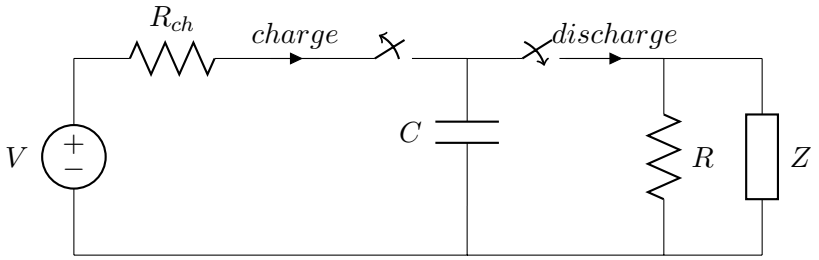


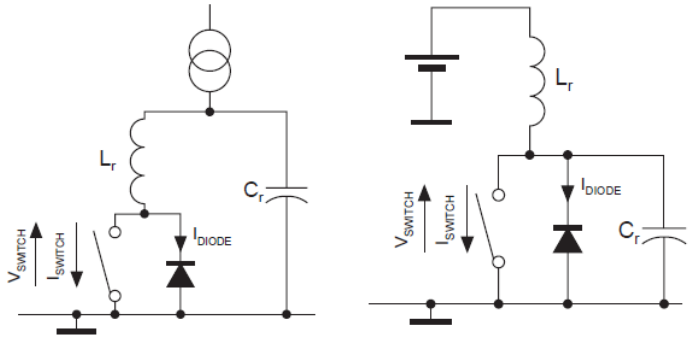
Figure 2.2 Capacitive discharge topology consisting of high voltage power supply V, storage capacitor C, time constant resistor R. The two states consist of charging and discharging

.

2.2.2 Resonant Converters

The advantage of using high frequency switching is reduced size and weight of components. However, switching losses are increased with increased frequency [Hart 1997]. Resonant converters use a capacitive and inductive tank to transfer energy to the load under resonance. This avoids switching losses that is associated with PWM controlled

topologies. A LC circuit can be designed to have either zero current switching (ZCS) or zero voltage switching (ZVS) where either the voltage or current is shaped across the switch. Both modes offer no dissipation across the switching device [Bildgen 2004].



(a) ZCS (b) ZVS

Figure 2.3 Resonant converter for a) zero-current switching and b) zero voltage switching [Bildgen 2004]

Figure 2.3(a) shows a zero-current switch. When the switch is closed, current flows from the capacitor to the inductor which follows a positive sinusoid waveshape. When the switched is open current flows through the anti-parallel diode, there exists no current during this state and therefore can be switched off without losses. For a zero-voltage switching design, in Figure 2.3(b), the switch will observe a linear increase in current flow from the inductor. When the switch is turned off energy flows into the capacitor from the inductor that follows a positive sinusoid shape. The switch is able to be turned on when the voltage of the switch finishes a positive half-wave cycle [Bildgen 2004].

The use of LC resonant converters is not idea for electroporation applications as a pulsed output waveform is not a square wave. It can be seen that the rise times are slow compared to the switching times. The load impedance is also required to be matched to the resonant converter to avoid reflections back from the load [Roche 2004].

2.2.3 Boost Converter Array

Boost converter arrays are designed similar to Marx generators; however, semi-conductor devices such as IGBTs are used as switching devices to improve operating frequency and operational life. The advantages of boost converter array are that high-voltage power supplies or pulse transformers are not required. Boost array converters only can produce unipolar pulses. Open circuit failure of one or more device generally does not lead to complete system failure. The structure is simple and can be used in conjunction with IGBTs with large current and voltage capabilities [Baek et al 2002]. However, as with capacitive discharge topology it suffers from low repetition rate capability.

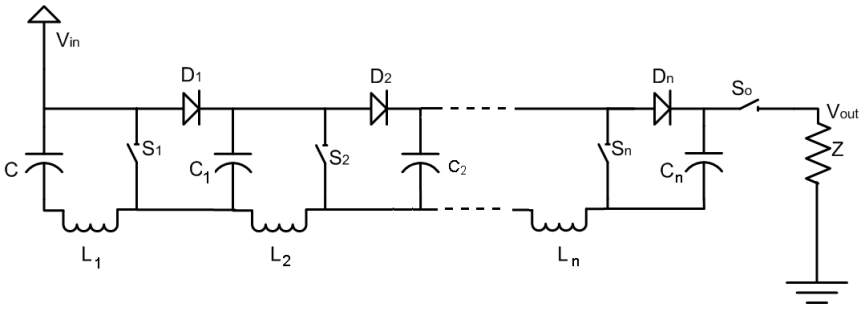


Figure 2.4 Boost converter design using a IGBT switching devices, output voltage is dependent on the number of series capacitors. [Baek et al 2002]

As in Figure 2.4 the capacitors are charged almost to the supply voltage when switches are turned off. The switches are turned on simultaneously to produce an output voltage proportional to the number of capacitors placed in parallel.

2.2.4 Full-Bridge Inverter

The H-Bridge, or full-bridge inverter, consists of at least four switches which alternate opening and closing. One suitable device for electroporation applications is the power MOSFET as it provides fast switching speeds and large current capability. Higher repetition rates and longer life can be achieved. It is common for the use of MOSFETs in biotechnology and medical applications [Grenier and Kazerani 2008]. The full-bridge inverter can produce positive and negative potentials, which are derived from a single DC supply source. As shown in Figure 2.5, the H-bridge design is arranged in an H shape. S1-S4 are blocks representing a switching unit. Switches S1 and S2 is referred to as the left-hand switching leg and forms the *half-bridge* arrangement. Conversely, S3 and S4 are referred to as the right-hand switching leg. N-channel type MOSFETs are normally used as the switching devices for power supply applications as they have a much smaller on-resistance, higher speed and lower price [Balogh 2001]. Using an N-channel MOSFET for the high-side switch requires gate dive circuity referenced to the source terminal. It is ideal that both the left side and right sides of the H-bridge configuration are identical so that current and losses are balanced [Rashid 2003]. The driving signals need to be taken into careful consideration which affects the output wave shapes, and which can also lead to switch failure and/or power supply failure.

The basic MOSFET switch model is shown in Figure 2.6, consisting of a switching device and a parallel diode. When current is flowing through the switch, there is some inductive energy. When the switch is turned off, the inductive energy, residing in either parasitic elements or inductive loads will create a negative voltage on the source terminal that could damage the MOSFET [Fairchild Semiconductor 2008]. Typically an external diode or *freewheeling* diode is added in parallel to the MOSFET body

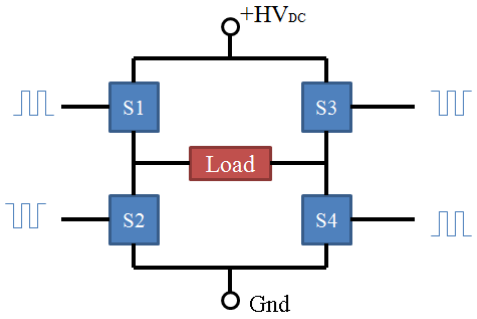


Figure 2.5 Full-bridge or H-Bridge topology

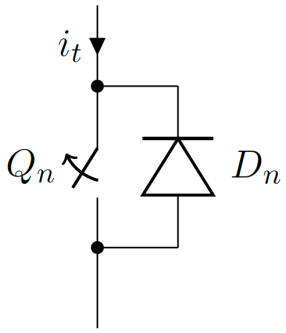


Figure 2.6 MOSFET switch device used in power electronic devices

.

diode to provide current path for the inductor energy. The combination of Q and D (including any added freewheeling diode) makes up the switching unit of block S.

When using MOSFETs, oscillations or ringing can occur due to parasitic elements. To mitigate this noise, gates can be terminated with gating resistors or with ferrite beads forming LC resonant networks [Dodge 2004].

As shown in Figure 2.7, the gate drive signals for S1, S2, S3 and S4 are pulsed simultaneously in such a way to alternate the DC voltage potential across the load. The switch pairs S1 and S4 are turned on at the same time while S2 and S3 are turned off to produce a positive load voltage across the load as in Figure 2.7 (a). After some period S1 and S4 are turned off and S2 and S3 are turned on as in Figure 2.7 (b).

If S1 and S3 or S2 and S4 are turned on at the same time; *shoot through* or *cross-conduction* can occur in which the power supply is effectively short circuited as in Figure 2.8. High pulsed currents can occur through cross-conduction that can exceed MOSFET drain-source specifications. Dead-time is therefore introduced between switching devices of each switching leg to mitigate shoot through currents. High-power full-bridge designs require longer dead-time due to increased parasitic elements [Chen and Peng 2008].

Table 2.1 lists the output states for a single H-bridge stage.

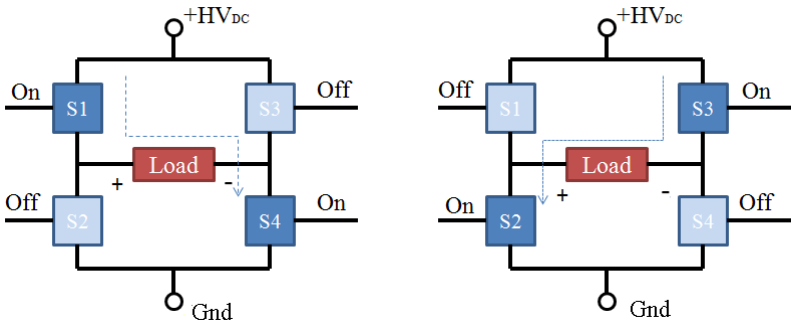


Figure 2.7 H-Bridge normal modes of operation with switches as in Figure 2.6, arrows indicating direction of current flow a) positive current flow across load b) negative current flow across load

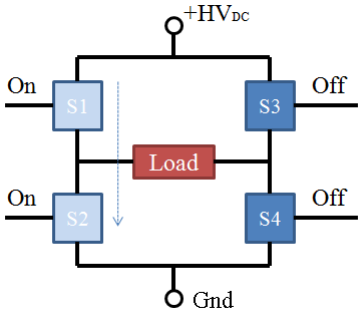


Figure 2.8 Illustrative example of shoot through current occurring when both switching devices of any switching leg are in a conducting state, this gives rise to significant power usage, device failure and distored waveforms.

Table 2.1 Switching signals for a single stage H-bridge. [Rashid 2001]

State	V_o	*Components Conducting*
Q1, Q4 on and Q2, Q3 off	$+HV_{DC}$	Q1, Q4 if $I_o > 0$ D1, D4 if $I_o < 0$
Q2, Q3 on and Q1, Q4 off	$-HV_{DC}$	Q2, Q3 if $I_o > 0$ D2, D3 if $I_o < 0$
Q1, Q3 on and Q2, Q4 off	0	Q1, D2 if $I_o > 0$ S3, D1 if $I_o < 0$
Q2 and Q4 on Q1 and Q3 off	0	D1, Q4 if $I_o > 0$ Q2, D4 if $I_o < 0$
Q1,Q2,Q3,Q4 off	$-HV_{DC}$ $+HV_{DC}$	D2, D3 if $I_o > 0$ D1, D4 if $I_o < 0$

2.2.4.1 Cascaded Configuration

The cascaded H-bridge configuration has seen vast applications in power generation specifically around DC-AC conversion for motor drive systems, power distribution and power conditioning applications [Alexander 2009]. Cascaded or multilevel H-bridge design is the idea of connecting several fullbridge designs to produce a multilevel output profile. It gives the ability of increased output voltage rating while using a series of

Table 2.2 Output voltage states for a two stage cascaded H-Bridge design

State	V_{output}	Stage 1 Output	Switches On	Stage 2 Output	Switches On
1	0	0	S1,S3 or S2,S4	0	S1,S3 or S2,S4
2	+E	+E	S2,S3	0	S2,S4
3	+E+F	+E	S2,S3	+F	S2,S3
4	-E	-E	S1,S4	0	S1,S3
5	-E-F	-E	S1,S4	-F	S1,S4
6	+F	0	S1,S3 or S2,S4	+F	S1,S4
7	-F		S1,S3 or S2,S4	-F	S1,S4
8	+E-F	+E	S2,S3	-F	S1,S4
9	-E+F	-E	S1,S4	+F	S2,S3

lower voltage devices. The disadvantage of a multilevel configuration is that it requires more switching devices and increasing control complexity [Kang et al 2004]. Table 2.2 shows the nine possible output voltage states for a two stage cascaded design given two power supply voltages with stage 1:H_{DC1} = E and stage 2: H_{DC2} = F, through the configuration shown in Figure 2.9. For the output profile illustrated in the previous Chapter(Figure 1.5), only states 1-5 are required.

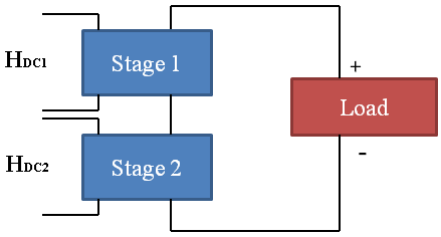


Figure 2.9 Block diagram of cascaded two stage configuration consisting of two isolated power supplies of H_{DC1} and H_{DC2}.

The cascaded H-Bridge configuration requires a π switching technique that is illustrated in Rashid [2003]. Each fullbridge stage consists of an isolated floating high voltage power supply. As fullbridge stages are cascaded together, each stage must conduct the full load current. Each power supply must also handle the load current. During a full commutation cycle, both high-side switches are turned on at the same time as well as both lowside switches sometime later. Each stage should conduct for 180° of a full cycle. This is to ensure that current is able to flow through ajacent stages that are turned off. With the π switching technique, the power losses are equal across all switching devices [Rashid 2003]. Each fullbridge stage has three output voltage levels derived from its power supply: $+V_{DC}$, $-V_{DC}$ and 0.

Figure 2.10 (a) illustrates a two stage cascaded design consisting of floating power supplies of HV_{DC1} and HV_{DC2} for stages 1 and 2 respectively. State 4 is shown in Figure 2.10 (a) with stage two conducting current derived from its power supply while

stage two conducts this current through S1 and S3. As a result, an output voltage of $-HV_{DC1}$ is seen from the load. State 5 is shown in Figure 2.10 (b), assuming equal power supply voltages for both stages, $-2HV_{DC}$ is seen at the output.

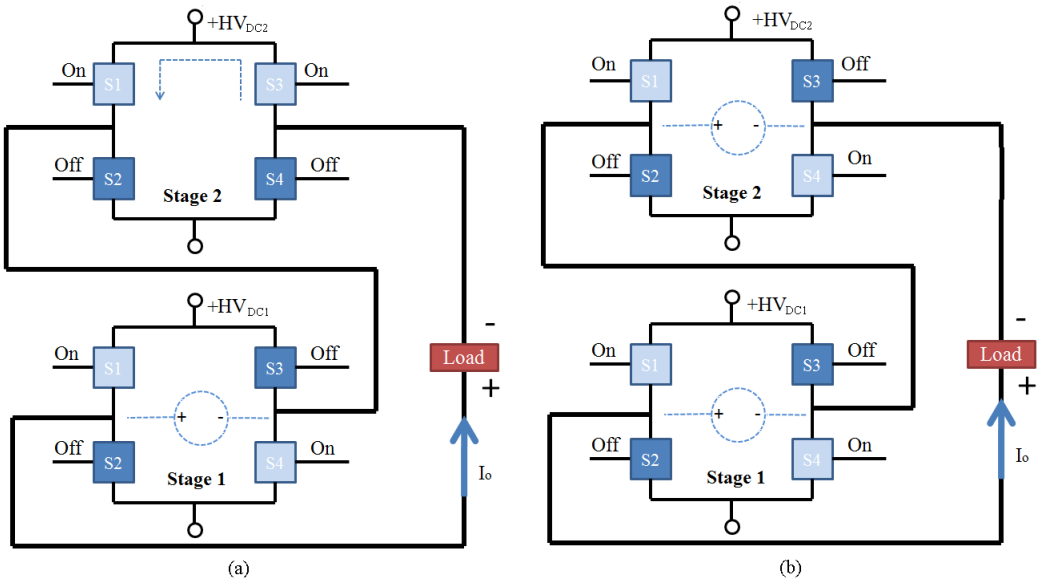


Figure 2.10 Illustrative example of a cascade configuration with a) state 4 and b) state 5 (as from table 2.2), giving output voltages of HV_{DC} and $2HV_{DC}$ respectively, assuming equal high voltage power supply voltages.

The number of output levels and the number of switches can be calculated for a given staggered staircase output profile. Given number of stages for multilevel inverter, the number output levels is given by equation 2.1. N_s are the number of stages and m are the number of output levels achievable. The number of switches required is given by equation 2.2, where l is the number of switches required [Wu 2006]. For a five level output design this requires two stages with eight switching devices, hence eight control signals. Both equations only valid for a π switching scheme.

$$m = 2N_s + 1 \tag{2.1}$$

$$l = 2(m - 1) \tag{2.2}$$

2.3 PULSE CONTROL SIGNALS FOR H-BRIDGE DESIGNS

2.3.1 Single H-Bridge Configuration Pulse Signaling

For single stage H-bridge designs a control technique similar to motor control is used whereby switching devices are turned on only when needed. For symmetric AC pulses, duty cycles of less than 50% is achieable; however, this does not allow for cascading as

no switcing devices will be in a conducting state duiring off periods. This is a simplistic design and requires only two separate driving signals. As illustrated in Figure 2.11, Q1, Q2, Q3 and Q4 are the control switching waveforms for a single fullbridge stage. In this scheme, Q1,Q4 use the same control signals and are switched on simultaneously as are switches Q2,Q3.

Prevention of cross-conduction is handled with sufficient dead-time though each switching leg. This delay has a bearing on performance depending on switching frequency and characteristics of the devices.

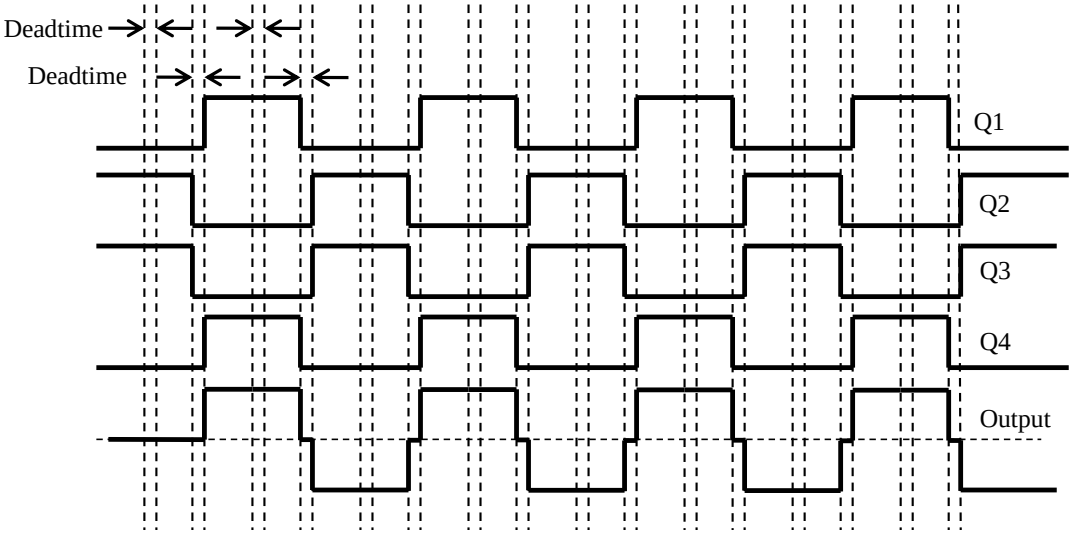


Figure 2.11 Switching waveforms for single stage design with 50% duty with assocated dead-time between switching devices.

A small portion of the output waveform, equal to the deadtime, will be seen between positive and negative switching cycles. This period should be significantly smaller than the pulse period to avoid waveform distortion.

2.3.1.1 Cascaded Configuration Pulse Signaling

For DC-AC power converters producing quasi-square waves a π switching technique is used outlined in Rashid 2003. This is adapted to suit a bipolar five level signal generator. Regardless of the duty cycle of the stage each switching device conducts for 180°. Each H-bridge uses a phase shifted waveform for switching timing. Figure 2.12 shows the switching technique used to achieve a cascaded output with balanced voltage steps (a non-symmetrical waveform shape however is desirable and will be explained in Chapter 5). During the state of zero output, either Q1,Q3 or Q2,Q4 are turned on simultaneously. This enables stages to be cascaded together allowing each stage to

pass current through during any on period. As a result, current stresses are balanced throughout all switches.

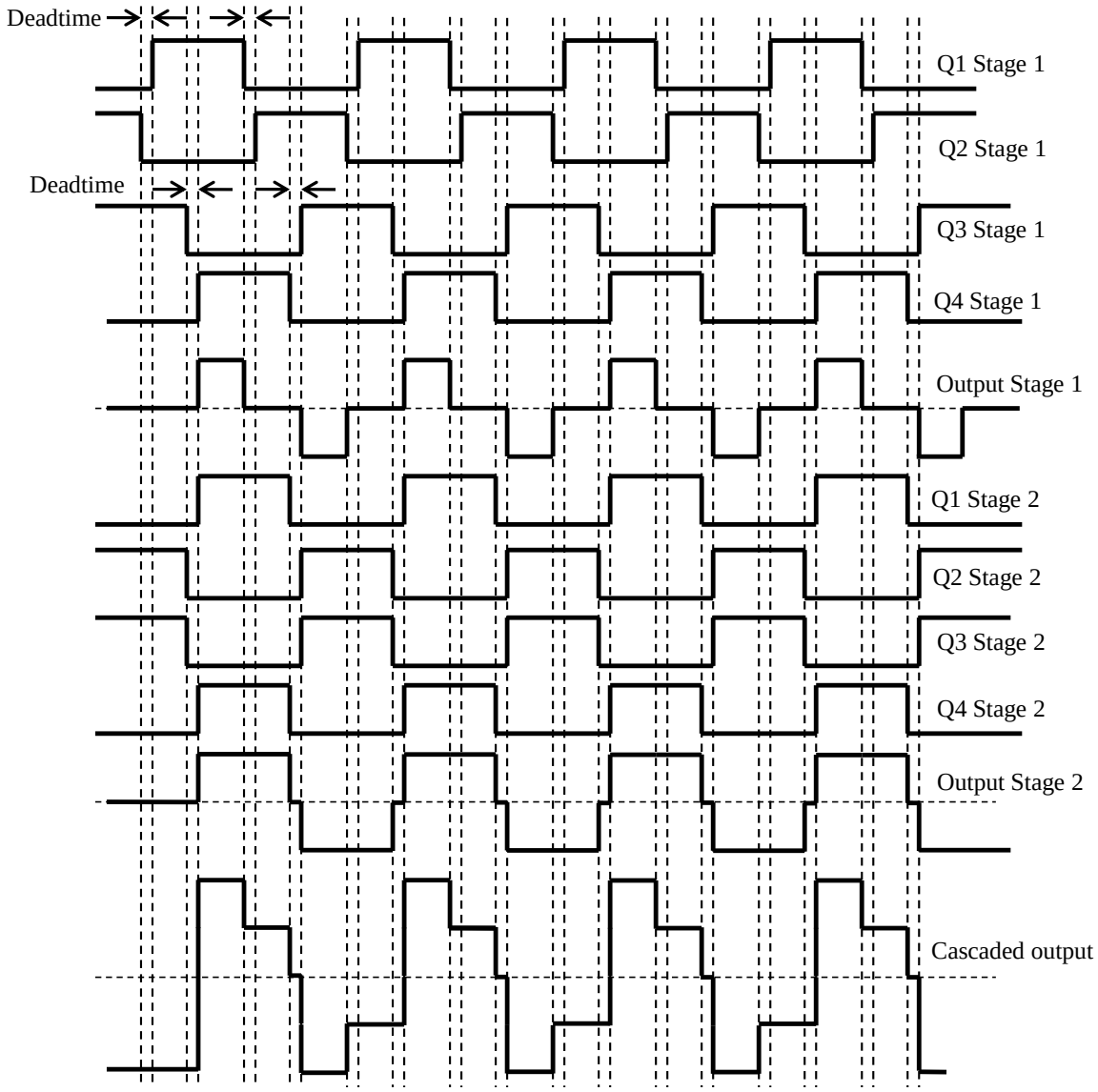


Figure 2.12 Switching waveforms for a two-stage cascaded B-bridge design with a symmetrical waveform, 25% duty for stage 1 and 50% duty for stage. Associated dead-time for switching devices is shown.

2.4 SUMMARY

This chapter has illustrated some of the semiconductor switching devices used for high-voltage and high frequency switching. Power MOSFETs are useful as the device operating frequencies are most suitable for electroporation purposes. However, IGBT's exhibit larger switching voltage capabilities with slower rise times compared to MOSFETs. For a pulse generator based on MOSFET switches with high voltage specifications of greater than 1 kV, cascaded H-bridge design is deemed most suitable. The Pi switching scheme was outlined for controlling a two stage cascaded H-bridge design.

Chapter 3

DEVICE CHARACTERISTICS

The selection of components for a pulse generator is paramount for the reliable operation in high voltage switching. MOSFETs will be used for the switching device because of their fast switching capability and large blocking voltage capability. Due to the MOSFETs significant input capacitance, MOSFET drivers with high pulse current capability are required for fast switching speeds. Design of a high-side driver is required as it is referenced to a floating node.

In this Chapter, switching characteristics of power MOSFETs are discussed and how switching performance is limited. Various techniques for driving the high-side switching device are explored. Isolation is also important in high-voltage designs, not only for safety, but also for noise issues that can affect pulse generator performance. Optocouplers and transformers are both devices used for isolation and level shift of the high-side switch.

3.1 POWER MOSFET SWITCH

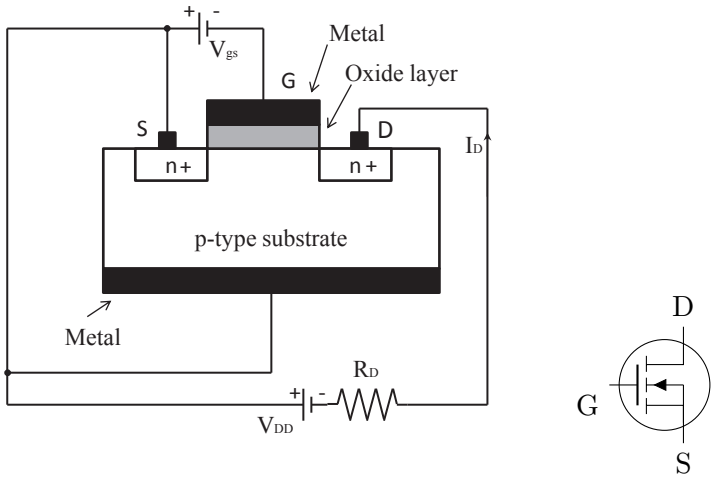
For electroporation applications, high-voltage, high-current and fast switching is required. These parameters in the device are important for designing a pulse generator. Performance factors such as efficiency, power capability, and reliability are dependent on the MOSFET switch selection. As seen in Chapter 2, MOSFETs are ideal for high frequency and high current capability; however, they have lower breakdown voltages compared to other power switches. MOSFETs exhibit low control requirements, fast switching transitions and low on-state resistances and are suitable for high-voltage and high-current pulsing. Current on-going developments in MOSFETs have led to greater blocking voltages, greater power capability, and decreased on-state resistances [Chaney and Sundararajan 2004].

3.1.1 Basic Structure

N-channel MOSFETs are fabricated through heavily doping n+ regions on a p-type substrate. The two basic types are depletion type and enhancement type. N-channel

enhancement MOSFET consist of n+ regions for the drain and source on a p-type substrate as seen in Figure 3.1. Metal contacts connect the drain and source terminals to the substrate. A silicon oxide layer exists between the metal gate terminal and drain-source substrate to provide isolation. For N-channel depletion type MOSFETs, N-type material is used to act as a conductive channel between drain and source. However, enhancement type MOSFETs do not have a channel. Instead, a layer of electrons (inversion layer) is formed on the oxide layer if there is a positive gate-source voltage. As depletion type MOSFETs are normally in a conducting state at zero gate voltage, negative gate-source voltage is required for a OFF-state. Enhancement type MOSFETS are therefore normally used in power electronic devices [Rashid 2003].

A MOSFET can be modelled with a parasitic BJT that exists between drain and source. An intrinsic body diode is formed between the drain and source as a consequence of shorting the base-emitter resistance through metalization [Rashid 2003]. This prevents the parasitic BJT from turning on; however, excessive dv/dt of the drain and source during turn off can still force the MOSFET into conduction [Oh 2000].



(a) N-channel enhancement MOSFET (b) Symbol

Figure 3.1 N-channel enhancement MOSFET (reproduced from [Rashid 2003])

3.1.2 Operational Theory

The gate-source voltage V_{gs} controls current flow from the drain and source terminals. When a positive voltage is applied to the gate of a N-Channel MOSFET (relative to the source), electrons are attracted from the p-type region to the metal oxide layer. This creates a conductive channel or accumulation layer in which the drain current i_d is able to flow through the drain to source resistance R_{ds}. Significant drain-source current can flow when V_{gs} reaches a threshold voltage V_{th}.

Large currents can also flow if avalanche breakdown occurs whereby the drain-

source voltage is exceeded and is clamped [Young 2004]. This can occur during excessive drain-source over voltages exceeding device parameters.

3.1.3 Output Characteristics

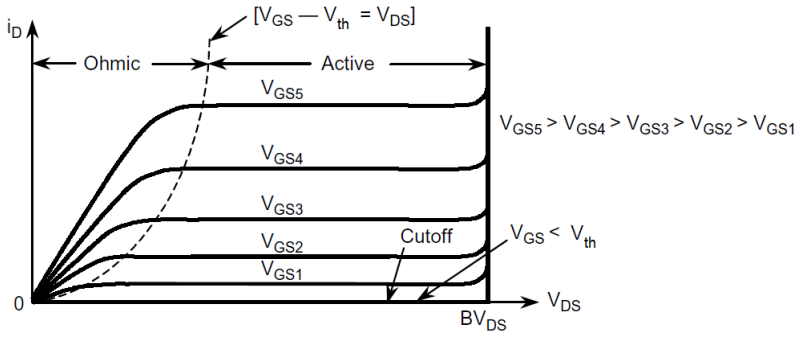


Figure 3.2 Output transfer characteristics (reproduced from [Oh 2000])

MOSFETs during switching operate in three modes: *cutoff*, *active* and *ohmic* regions as illustrated by Figure 3.2. As in Rashid [2003] and Mohan et al [2003], the cut-off region is when the MOSFET is turned off with the condition $V_{gs} \leq V_{th}$, no current flows between drain and source. The device must block the drain-source V_{ds} voltage. The drain-source voltage must not exceed the drain-source breakdown voltage BV_{ds} of the device or else avalanche breakdown can occurs alongside high power dissipation. For the MOSFET to fully turn on, the MOSFET moves from the cutoff region, though to the active region, and then to the ohmic region. The active region is reached when $V_{ds} \geq V_{gs}$ - V_{th}. The active region is where the switching action of the MOSFET occurs, hence where switching losses mostly occur. In this region, the drain current is proportional to the gate-source voltage. It is ideal that the MOSFET spends as little time as possible in this region. Due to the Miller effect, the rise and fall time of the gate-source voltage can become progressively longer extending the time spent in the active region. In the ohmic region, where $V_{ds} \leq V_{gs}$ - V_{th}, the MOSFET is in a on-state and in a constant resistance region. High drain current i_d flows with small drain-source voltage and is proportional to the drain-source voltage.

3.1.3.1 Switching Characteristics

The equivalent circuit, with parasitic elements contributing the greatest effect on switching performance for the MOSFET is shown in Figure 3.3. The source inductance L_s and drain inductance L_d are associated with the package configuration.

The parasitic capacitances of MOSFETs limit the switching capability. MOSFETs usually have gate capacitances (C_g) less than 1 nF. It is the major limiting factor to

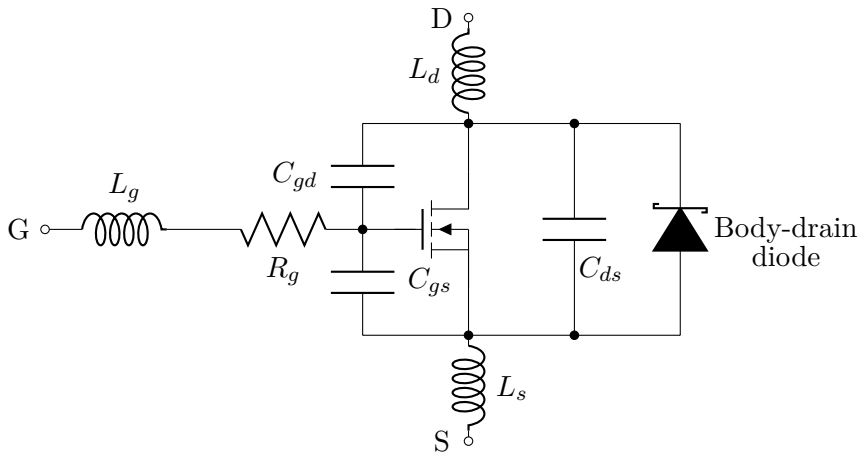


Figure 3.3 Major parasitic element of the MOSFET that cause noise.

switching performance. They are characterised by: input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss}. The parallel combination of the gate-drain capacitance (C_{gd}) and the gate to source capacitance (C_{gs}), is referred to the input capacitance, with $C_{iss} = C_{gd} + C_{gs}$. C_{gd} and C_{gs} are determined by the geometry of the device. The output capacitance is given by $C_{oss} = C_{gd} + C_{ds}$. The reverse transfer capacitance is given as $C_{rss} = C_{gd}$. C_{ds} is determined by the parasitic body diode. Current through the gate-drain capacitance C_{gd} is related by Cdv/dt, therefore large voltage gain of the MOSFET results in significant reverse transfer capacitance. The majority of the problems of high-speed switching is through charging and discharging the input capacitance [Oh 2000, Balogh 2001].

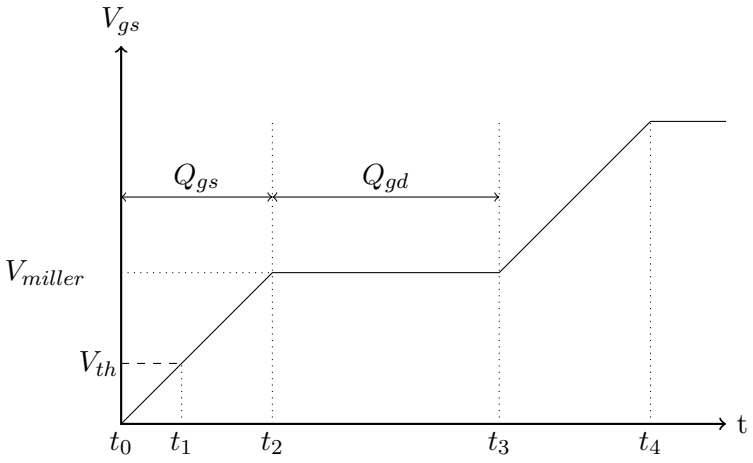


Figure 3.4 Typical MOSFET gate drive charging characteristics

Faster switching speed can be achieved through charging and discharging the gate capacitor as fast as possible through external circuitry. When considering gate driver requirements, total gate charge specifications are considered. Figure 3.4 shows the gate

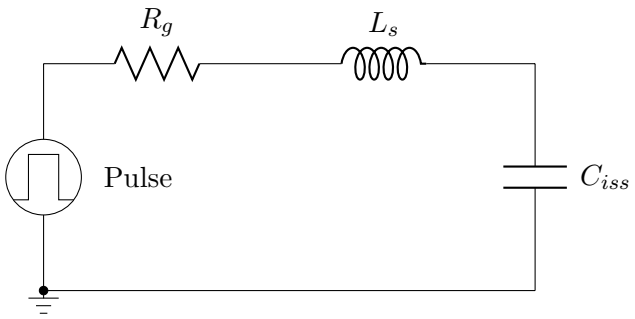


Figure 3.5 Equivalent gate circuit creating a series RLC network

voltage V_{gs} transition for turn-on of the MOSFET. During turn on, from t_0 to t_1, the gate-source capacitance is charged to the MOSFET threshold voltage. After this point the MOSFET is able to conduct current. From t_1 to t_2, V_{gs} continues rising and reaches the Miller plateau. For a diode clamped inductive load, during this time, the drain current rapidly rises. The drain-source voltage V_{ds} starts to drop from periods t_2 to t_3 as the gate-drain capacitance C_{gd} or Miller capacitance is charged. After period t_3, the MOSFET is conducting with only conduction losses, drain current i_d is determined by V_{gs}. Q_{gd} is the Miller charge, this is the major charge that is responsible for limiting switching times [Oh 2000].

The turn-off sequence of the MOSFET is the reverse of turn-on, where parasitic components are discharged to ground.

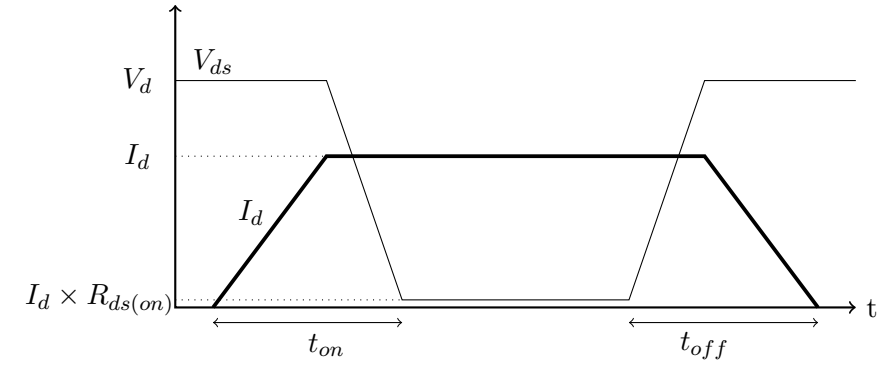
Charging and discharging of the gate can also be considered as using an equivalent RLC circuit, as shown by Figure 3.5 [Balogh 2001]. The series combination of gate resistance R_g, source inductance L_s and C_{iss} forms a resonant network in which oscillatory spikes can be observed on the gate drive during switching. During turn-on, the gate current flows through a L_s and consequently slows down turn-on time.

Significant voltage can also seen across the source inductance during periods of high di/dt drain current. This has an effect of negative feedback. This can occur when the gate drive is between V_{th} and V_{miller}, or regions t_1 to t_2 with high change of drain current, as in Figure 3.4. High voltage across the source inductance results in reduced voltage across the gate drive, and as a consequence di/dt is reduced.

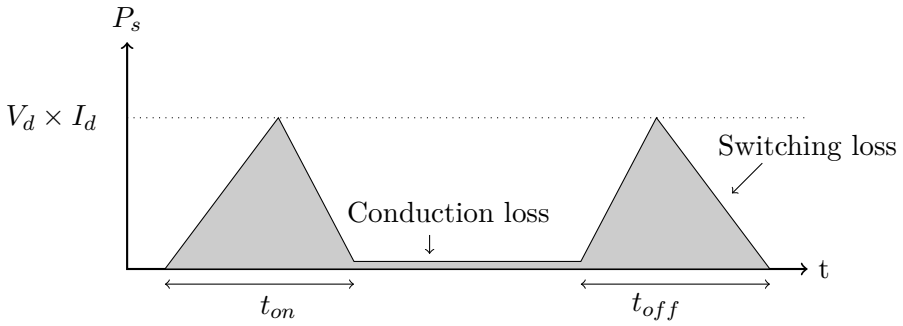
The drain inductance of Figure 3.3 limits di/dt at turn-on and can be beneficial at reducing switching losses. However, at turn-off, as the drain current drops the resulting voltage across L_d causes overshoot of V_{ds} causing greater switching losses [Balogh 2001].

Inductive elements arise from PCB layout and switch device interconnections. For example SO8, DPAK, D2PAK and IPAK have varying source inductance L_s between 1.5 nH and 7 nH. Smaller source inductance will cause shorter rise and fall times. The combination of inductive and capacitive elements gives rise to *ringing* noise that is an issue with high-speed switching devices [Elbanhawy 2008] [Balogh 2001].

3.1.3.2 Power dissipation



(a) Turn on and turn off drain-source voltage and drain current



(b) Power loss due to switching and conduction

Figure 3.6 Switching losses of a MOSFET

As shown in Figure 3.6(b) (a) and (b), total power losses are contributions of switching losses and conduction losses. Switching losses in the MOSFET is proportional to the switching frequency and the turn-on/turn-off times.

The power loss due to switching can be estimated with equation 3.1 [Shen et al 2006].

$$P_s = (1/2)V_d I_d f_s t_{c(on)} + t_{c(off)} + (1/2)C_{oss}V_d^2 f_s \tag{3.1}$$

where V_d is the drain-source voltage, I_d is the drain current, f_s is the switching frequency of the MOSFET, and $t_{c(on)}$, $t_{c(off)}$ are the specified turn-on and turn-off times of the MOSFET . The first term relates to $t_{c(on)}$ and $t_{c(off)}$ where overlap of drain current and drain-source voltage can be observed. This is the main switching loss. The second term relates to the output capacitance discharging through the MOSFET channel [Shen et al 2006].

The power loss due to the MOSFET resistance during a on state is given as:

$$P_{on} = R_{DS(on)}{I_o}^2 \tag{3.2}$$

where $R_{DS(on)}$ is the on-state resistance and I_o is the steady current.

As the MOSFET is turned on, the drain current starts to rise. After a set amount of time referred to as the turn on time $t_{d(on)}$ the MOSFET drain-source voltage starts to drop. This is the time required for C_{gs} to charge up so that the threshold voltage V_{th} is exceeded turning the MOSFET on. When there exists both drain current and drain-source voltage switching loss occurs. The total delay time to turn the device on is taken as 10% of V_{gs} voltage to 10 % of V_{ds} voltage.

3.2 MOSFET DRIVERS

Specifically designed MOSFET gate drivers provide the necessary sourcing and sinking of the MOSFET gate current during switching. It must switch between the full voltage range to fully turn the MOSFET on where conduction losses are low. It is ideal that the MOSFET spends minimal time in the active region as this is where power dissipation is large. The drive circuit must provide enough gate current so that turn-on and turn-off times are minimised while still with acceptable switching losses [Mohan et al 2003].

MOSFET gate drivers are implemented through transformers, integrated circuit (IC), and discrete components. Various manufacturers produce gate drives that provide gate isolation, protection, and control functions [Mohan et al 2003]. Many manufacturers also provide IC drivers for half-bridge and full-bridge configurations. This reduces the control signal complexity. A hardware controlled dead-time solution, to prevent cross-conduction, is often used for half-bridge and full-bridge configurations. However, for specific applications single output gate drivers are used so efffects of ringing through PCB layout can be managed. For switching at high-speed: propagation delay, quiescent current, latch-up immunity and driver current limitations, are aspects taken into consideration when using drivers [Dunn 2004].

3.2.1 Operational Theory

The MOSFET gate has significant capacitance that can give rise to high peak currents when switching. As a result, the gate is a low impedance input for switching transitions and a high impedance input during on and off periods. It is therefore ideal that the driver has a very low output impedance to provide high peak currents. To achieve switching speeds less than 100 ns, a totem-pole gate drive configuration can be used as in Figure 3.7. A NPN-PNP transistor pair is used to create a push-pull configuration. During turn on, the comparator turns the NPN transistor on, charging up the gate capacitance through R_g. During turn off, the PNP transistor short-circuits the gate to ground, discharging the gate charge through R_g. A suitable gate resistor R_g is determined, as to reduce electro-magnetic interference (EMI) that reduces switching performance. On the contrary switching losses are larger for large gate resistors. By reducing the pulsed current to the gate, this reduces the charge and discharge rate by

slowing down switching times. As a result dv/dt, di/dt is reduced. Voltage spikes that are caused by stray inductances in the circuit can be reduced using a suitable gate resistor and through snubbing.

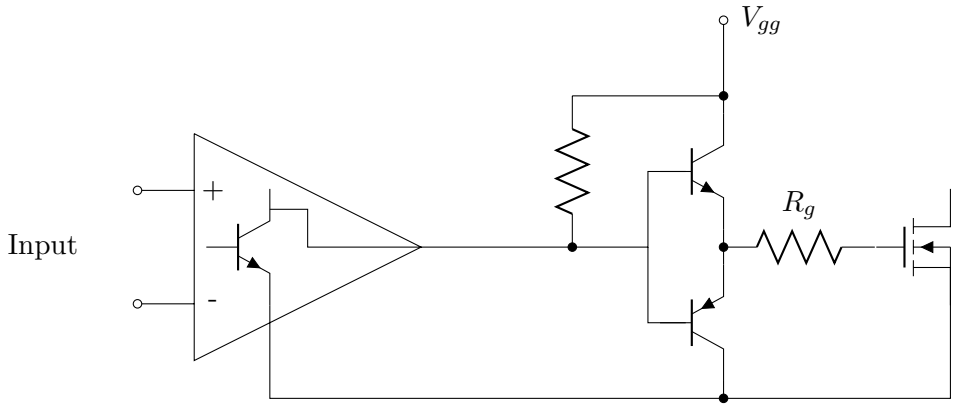


Figure 3.7 Bipolar totem pole noninverting MOSFET driver using discrete components

The power dissipation of the MOSFET driver is determined by the charging and discharging energy of the switch [Dunn 2004]. It can be seen by the equation:

$$P_d = C_g V_{gs} f_s \tag{3.3}$$

3.2.2 High-Side Gate Drive Power Source Requirements

As explained in the previous Chapter, the high-side switch requires a driver that is located on a *floating node*. It is desirable that the driver has all the usual characteristics of sweeping between the full voltage range, switching at fast speeds, using minimal power, and exhibiting low propagation delay. However, the floating node situation requires an isolated power source solution. Various techniques are explained in Rashid [2003], International Rectifier [2007] and Fairchild Semiconductor [2008]. These include:

- Floating gate drive power supply
- Transformer coupled drive
- Charge pump
- Bootstrap
- Carrier Drive

3.2.2.1 Floating gate power supply voltage

A floating gate supply is the simplest method; however, it requires independent power supplies for both high-side switching devices. Figure 3.8 illustrates the floating supply

method, A and B are separate floating power supplies. For a fullbridge design, both low-side switches are referenced to the same node, therefore; they can use the same gate drive power supply (C).

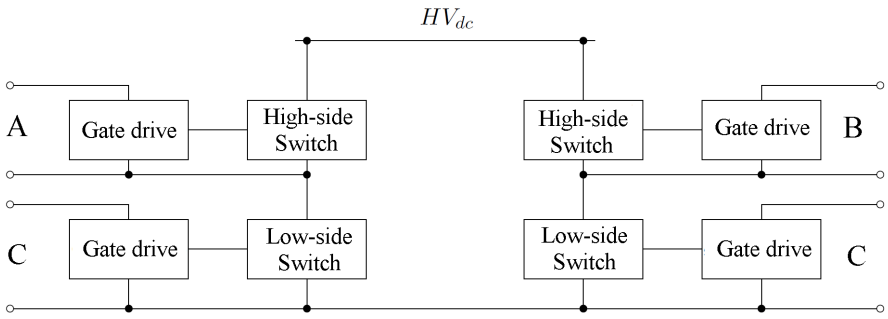


Figure 3.8 Floating gate drive supply for a fullbridge inverter

3.2.2.2 Pulse Transformers

Traditionally, pulse transformers were used for high-side gate drives. Gate driving as well as isolation of the high-side switch can be achieved by a pulse transformer using minimal PCB area. However, significant turn-on and turn-off delays are seen [Balogh 2001]. Pulse transformers are normally used for isolation; they are useful for producing square wave pulses over a finite bandwidth. Since the transformer has a finite amount of energy storage, duty cycles are limited. Long pulses at low switching frequencies can lead to transformer saturation. The use of pulse transformers is cost effective with the transformer size decreasing with increasing frequency [Rashid 2003] [Locher 1988].

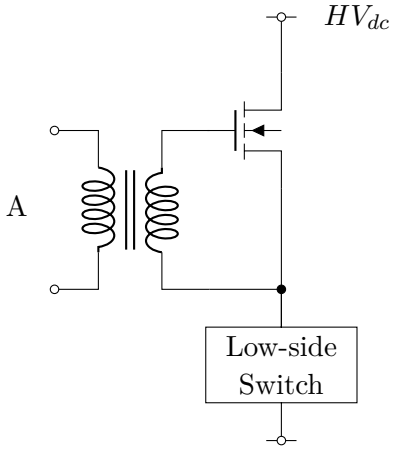


Figure 3.9 Single ended pulse transformer for high-side switching device

Ideally, the transformer should couple the primary and secondary windings with all energy being transfered. Minimising leakage inductances, magnetizing inductance

and coupling capacitance is desirable as it can cause distortion such as phase-shift, timing error and overshoot. High coupling capacitance between primary and secondary windings is associated with non-uniform winding layout and excessive number of turns in the primary/secondary windings [Scoggins 2007]. Figure 3.9 illustrates a use of a pulse transformer for the high-side switching device.

3.2.2.3 Bootstrapping

Bootstrapping is a useful technique as it is simple to design and inexpensive [Rashid 2003]. The downside to bootstrapping is that negative voltages can still occur at the source of the high-side device that is associated with inductive loads [Merello et al 2005]. The bootstrap requires a diode D_{bs} and capacitor C_{bs} as shown in Figure 3.10. When the low-side switch is turned on, the bootstrap capacitor C_{bs} charges to V_{cc} volts through the resistor and diode. The low-side MOSFET switches off some time later sufficient for the capacitor to charge. When the low-side MOSFET is turned off the high-side top rail of the driver will be seen at $V_{cc} + V_{dd}$ volts referred to ground. A suitable size capacitor is required as the capacitor needs to charge and discharge fast enough to maintain supply to the high-side driver.

To determine the bootstrap capacitance value, the gate charge requirement is calculated from equations 3.4, 3.5 and 3.6 [Fairchild Semiconductor 2008]. Q_{gate} is the total charge of the gate, I_{LKCAP} is the leakage current of the capacitor, I_{LKGS} is the leakage current of the gate, I_{QBS} is the quiescent current of the boot-strap circuit, I_{LK} is the bootstrap circuit leakage current, $I_{LKDIODE}$ is the leakage current of the diode, t_{on} is the on time for the MOSFET and Q_{LS} is the charge required by the level shifter.

$$C_{bs} = Q_{total}/\Delta V \tag{3.4}$$

where Q_{total} is the total gate charge and ΔV is the allowable voltage drop on the bootstrap capacitor.

$$Q_{total} = Q_{gate} + (I_{LKCAP} + I_{LKGS} + I_{QBS} + I_{LK} + I_{LKDIODE}) \times t_{ON} + Q_{LS} \tag{3.5}$$

Determining the peak current for the gate is determined by the total gate charge and turn-on/turn-off time of the MOSFET:

$$I_{peak} = Q_{total}/dT \tag{3.6}$$

A high-speed diode is required to block $V_{cc} + V_{dd}$ volts as the power supply is referenced to ground. Hence, the diode should be selected to have a break down voltage greater than the high-voltage supply. Diodes with reverse recovery T_{rr} times

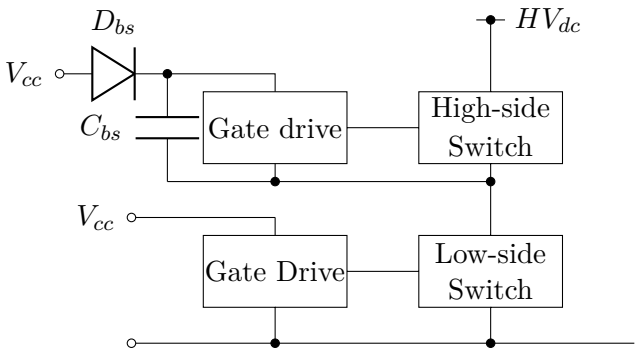


Figure 3.10 Bootstraping with bootstrap diode and capacitor

in the order of tens of ns are sufficient charging the bootstrap capacitor as to minimise any charge being fed back into the high-side power supply. The bootstrap capacitor is charged and discharged at a high speed with large dv/dt and di/di occurring therefore should be placed close to the driver [Fairchild Semiconductor 2008].

Negative voltage of the high-side source node occurs as the highside switch is turned off. The load current is turned off allowing current to flow through the freewheeling diode of the low-side switch. The amount of negative voltage is seen to be proportional to parasitic inductances associated with the lowside switch and change in current seen through the highside switch. The driver reference node for the high-side switch can be pulled significantly below ground. Negative voltage on the floating node can cause overvoltages of the bootstrap capacitor [Fairchild Semiconductor 2008] [Balogh 2001] [Meloncelli 2001].

3.3 CONTROL SIGNAL ELECTRICAL ISOLATION

The purpose of isolation is the electrical separation between high-voltage and low-voltage components. Digital control circuitry using CMOS logic levels are also separated from high-voltage switching noise through electrical isolation. A secondary purpose of electrical isolation is to provide a level shift for high-side switches. Opto electronics and transformers are two such methods of electrical isolation. The basic concepts transformer isolation are also valid for pulse transformers as discussed for diving a high-side switch.

3.3.1 Digital Isolation and Level Shift

Opto-couplers provide excellent transient immunity characteristics that occur in high-voltage switching. Shown in Figure 3.11 is the use of an optocoupler to couple signals referenced to two different ground planes. An input signal uses an LED and is forward biased. A complementary photo-transistor serves as an output following the input voltage. The output uses an open collector transistor. High voltage transients caused

by switching noise are isolated between separate grounds. The turn on and turn off time of photo-transistors are typically small [Rashid 2003]. For a highside switch on a fullbridge inverter, the output is referenced to a floating node. To avoid false turn on and turn off due to the different reference point at input and output, the LED and photo-transistor combination is encased inside a package with minimal capacitance between input and output [Mohan et al 2003].

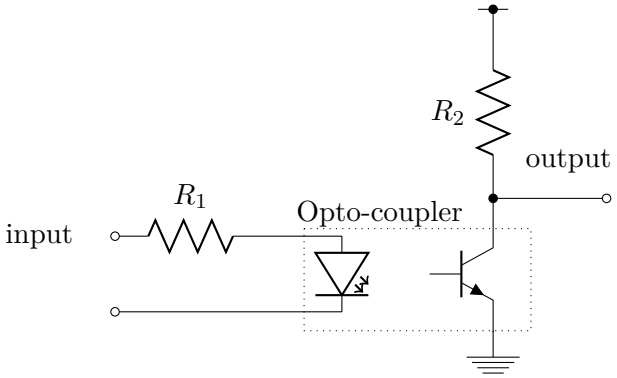


Figure 3.11 Typical Optocoupler configuration

Optocouplers are useful in that they are less susceptible to stray magnetic fields. They are typically rated to block common-mode transients of 50-30 kV/μs. Unlike transformers they do not suffer from capacitive coupling from input to the output [Hewlett Packard 2007].

Chapter 4

HIGH VOLTAGE SIGNAL GENERATOR DESIGN AND CONSTRUCTION

The operational theory of MOSFET behavior at turn-on and turn-off was described in Chapter 3. Methods of gate control were also outlined alongside high-side drive requirements. The design and implementation of a high-frequency/high-voltage signal generator is outlined in separate sections within this Chapter. This includes aspects of the digital control implemented to produce the required pulse signals and the cascaded H-Bridge design used to produce bipolar stepped waveforms. The choice of components is outlined, which are deemed suitable for the pulse generator. Construction of the pulse generator and control boards are also detailed alongside the challenges associated with noise generated from high frequency/high-voltage switching. This Chapter also illustrates methods used to mitigate noise associated with high-frequency/high-voltage switching. The testing methodology and results for the pulse generator are shown in the next Chapter.

A low-voltage (LV) full-bridge or *stage* was initially built to investigate H-bridge control requirements and MOSFET switching behavior. Later, two separate stages were built with higher power capability. A *high-voltage* stage, capable of producing up to 1000 V_p pulses, was combined with a *low voltage* stage able to produce pulses of up to 200 V_p. Each stage consists of separate isolated high voltage supplies and isolated power supplies for gating requirements, as explained in Chapter 3. Isolation, high-side switch control, and switch gating requirements are addressed. The use of a modular arrangement made the boards easier to test through various operational situations. Signal generation for H-Bridge control was provided by a separate control board using a MCU, this also provided a useful user interface.

To reduce high-frequency noise from MOSFET switching the following areas are addressed:

- Power supply decoupling is used to reduce conducted high-frequency noise from entering the circuit components. A range of capacitor sizes are used in parallel to decouple components so that a broad range of high-frequency noise is bypassed.

Ceramic capacitors are ideal for bypassing of high-frequency noise as they have a good frequency response. Tantalum capacitors are useful for medium to low frequency decoupling [Schmitz and Wong 2007]. Decoupling capacitors will help to reduce common-mode voltages that are coupled to the power supply [Hewlett Packard 2007].

- PCB layout is crucial for limiting noise sources. High frequency noise can arise from high impedance current loop paths from supply to ground pins [Balogh 2001]. Ground planes are ideally used to provide low impedance current return path for components. The full-bridge inverter is inherently an RCL oscillator which give rises to overshoot and ringing. Parasitic inductances can be most ideally limited by reducing PCB loop areas of high current which otherwise cause radiated switching noise. Cross-talk from high-frequency signals interfering with adjacent signals can cause false signaling and propagation delays. This can be reduced by using differential routing, short track length and routing signals orthogonal to each other on different layers [Karunakaran 2003].

- Placement of components have effects on parasitic inductance and propagation delays causing electromagnetic interference (EMI). EMI is an issue in power electronics that is both unpredictable and difficult to determine. Careful component placement by using short tracks and reducing loop areas is known to reduce EMI significantly [Joshi and Argarwal 1999].

4.1 HARDWARE DESIGN

A cascaded H-bridge topology (as outlined in Chapter 2) is used, as bipolar waveforms with fast rise and fall times can be produced using modern MOSFET switches. As the output frequency rises, the shape of the output waveform becomes distorted due to limitations in rise and fall slew rates and due to resonant excitation of parasitic elements. As such, desired waveforms become difficult to achieve above several hundred kHz. Switching noise or ringing becomes more apparent at higher frequencies which effects the desired application performance. Through careful PCB layout some of the effects of switching noise can be managed by reducing parasitic elements. Figure 4.1 illustrates the functional modules of the high-voltage pulse generator that were considered.

The pulse generator design consists of an open-loop configuration. The open-loop configuration is used for a simplistic design and to avoid layout difficulties. Short-circuiting of any switching leg still needs to be considered as there are no feedback sensors that can be used for fault detection. A closed-loop system is not necessary for the intended applications of the pulse generator. The high-voltage stage should function with power supply voltages of up to 1 kV_p while the low-voltage stage should be capable of switching up to 400 V_p, with a bi-polar waveform shape. In a cascaded

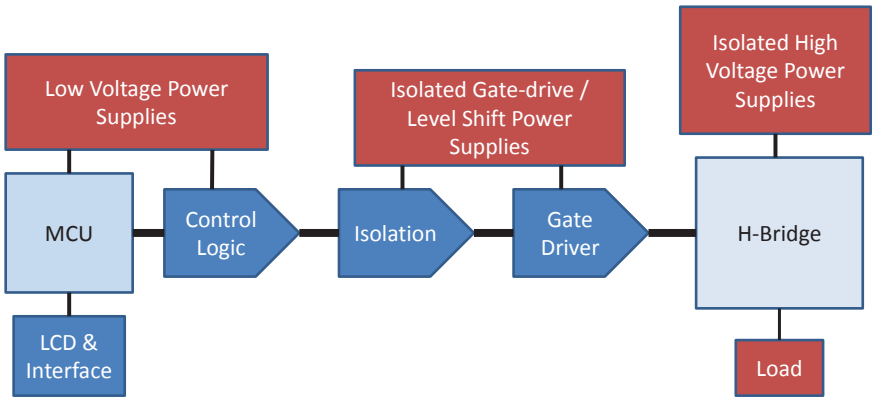


Figure 4.1 Pulse generator open-loop configuration with proposed design sections

design, both stages should be able to withstand the highest bridge current as both stages conduct the total load current. High-current MOSFET drivers are used to provide pulse current drive for switching MOSFETS at the fastest possible speed. Consideration of the drain-source voltage specification of the MOSFETs needs to be addressed for reliable performance. Signal isolation is used in the form of opto-couplers to prevent switching noise interfering with the digital control logic. Opto-isolation also is used in the level shift mechanism for the highside gate drivers. The control system providing the switching signal is produced on a MCU as it can be easily configured for different applications, given a suitable user interface. Variable dead-time delay can also be produced on a MCU which is more complex to produce in hardware.

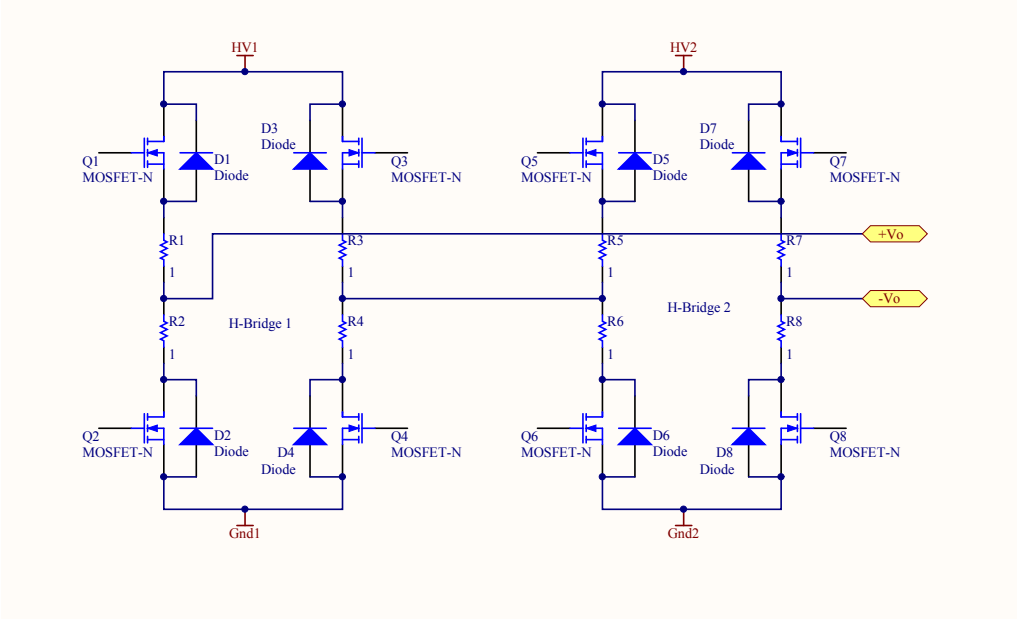


Figure 4.2 Cascaded fullbridge configuration. Load output at terminals +Vo and -Vo.

The basis of the cascaded full-bridge configuration (identified in Chapter 2) consists

of the design in shown in Figure 4.2. A bridging node between the two full-bridge stages connects the two stages in series. To limit possible shoot-through current, low inductance 1 Ω, 2512 series resistors are placed between each switching leg. However, this potentially increases the loop area of the load, increasing noise. The 2512 series resistors provide 1 W of power dissipation capability with maximum over voltage of 400V. Knowledge of the load specifications is desirable so these values are not exceeded. The output impedance of the full-bridge stage has also been increased as a result of adding current limiting resistors, reducing the pulse voltage amplitude at the load.

Given an opto-coupler with an open collector output, an inverted output can be provided using a pull up resistor. If the MOSFET driver is non-inverting, the digital control logic is required to be inverting in order to avoid overlap of switching devices on each switching leg. Alternatively, a non-inverting output can be provided by using a pull-down resistor on the emitter and tying the collector directly to Vcc.

For modularity, separate boards were designed for the high voltage switching side and digital control side. Ringing due to long traces will become more predominant; therefore, short signal traces were used.

FR-4 printed circuit board (PCB) laminate was used as it was the most readily available in the electrical engineering department. FR-4 is a low cost laminate with excellent insulating properties, the dielectric breakdown voltage is listed as 1100 V/mil [Ritchey 1999].

4.2 DIGITAL CONTROLLER FOR PULSE GENERATION

The four main forms for generation of control logic signals are: discrete logic, field programmable gate arrays (FPGA), digital signal processing units (DSP), and micro controller units (MCU). A MCU was chosen as it is easily configurable and can achieve pulse frequencies above several hundred kHz.

The ATmel AT90PWM2B [ATmel Cooperation 2006] was selected as the MCU for signal generation. It is an 8-bit device with 8 Kb of flash for programmable memory. This device has a dedicated power stage controller for pulse generation suitable for a single stage H-bridge design. The use of this function also allows the user to specify a dead-time. However, for a cascaded H-bridge design, using a π switching algorithm as outlined in Chapter 2, is required. For a two stage H-bridge design, 8 control signals are needed. Two control boards were built using the AT90PWM2B. The first one was used to assess the generation of pulse signals. The second was used for digital control generation and user feedback through a display.

The two functions for the MCU is to provide gate signaling for two H-bridge stages and to provide a configurable interface for electroporation research. Signaling is pre-formed using the MCU timer to set frequency, waveform shape, and dead-time. A

2x16 alphanumeric LCD display using the HD44780 controller, with a 4-bit interface, provides user feedback of: duty cycle ratio, frequency, pulse durations, and delay times of the output pulse.

The AT90PWM2B clock source is obtained from the phase-locked loop (PLL), this is divided down by four giving a maximum frequency of 16 MHz. Given this clock source, the time between each instruction is 128 ns (the minimum delay between changes on any output state). This is the limiting factor for timing operations of the pulse generator. The clock is further divided by 8, 64, 256 or 1024 to achieve a slower clock and thus lower switching frequencies. Two general purpose counters/timers are utilised on the AT90PWM2B. The 16-bit timer (Timer/Counter1) was used to produce digital logic signals, this gave a wider range of count values for a given clock source. The second 8-bit timer (Timer/Counter0) was used for non-critical timing tasks such as delays for LCD control and de-bouncing for button interface. Two 8-bit general purpose input/output (GPIO) ports were used, designated PORTB and PORTD. PORTB was used as the output pins; providing the eight independent signals for the pulse generator. PORTD was used for the LCD and button interface. Using a single I/O (Input/Output) port for both output stages gives the ability to switch output stages simultaneously with minimal delay.

The schematic for the control board is provided in Appendix A with Table 4.1 listing the output pins used.

Table 4.1 Output pin configuration for MCU control board

Outputs	*Description*	*MCU Pin*
Data 1-4	4-bit data bus for LCD interface, parallel connected ISP	PD0-PD3
R/S	Reset line pin for LCD	PD4
C/S	Reset for LCD	PD6
LV output	Stage 1, control signals	PB0-PB3
HV output	Stage 2, control signals	PB4-PB7

Power supply filtering for the MCU consisted of a tantalum capacitor and several 0604 series ceramic capacitors in parallel. This serves to bypass noise signals created during GPIO switching. Since a 5 V digital supply is required for the AT90PWM2B, a LM34801 voltage regulator was used to provide a reliable constant voltage. This provides maximum current output of 100 mA for a maximum input voltage of 35V. The maximum DC current for the AT90PWM2B is listed as 40.0 mA per I/O pin. Low current opto-couplers are ideal so that the power supply current of the MCU is not exceeded. The input was bypassed with bulk decoupling using 0.1 μF ceramic capacitors. This filters high frequency noise associated with the power supply.

Table 4.2 Input pin configuration for MCU control board

Inputs	*Description*
Reset	MCU reset line for programming connected on PE0, required to be tied at high state to prevent reset
Button 1-3	For user input located on PE1, PD6 and PD7

Programming of the AT90PWM2B consists of using the in-service programming lines. An AVR ISP programmer was utilised for uploading of program code onto internal flash memory. Tactile buttons were placed on PORTD and PORTE with 1 kΩ pull-up resistors to provide user input. Table 4.2 lists the input pins on the MCU.

4.2.1 Physical construction of the Control Board

The digital control board was built up on a FR-4 type printed circuit board. A parallel ground and power plane was used for the two layer board so as to reduce inductance and provide low impedance current paths. The ground plane will provide a common reference voltage in which high frequency signals can run over. By magnetic-field cancellation the inductance can be reduced [Ardizzoni 2005].

The AT90PWM2B draws a small amount of average current during switching. However, large current spikes may be present on the power supply during switching. Any rapid changes in current gives rise to noise. The magnitude of the noise is derived from the product of pulsed current and characteristic impedance (Equation 4.1).

$$\Delta V = \Delta I \times Z_o \tag{4.1}$$

As a single I/O port is used the current pulses may be a few hundred mA. Local decoupling capacitors mitigate this problem, the placement of the capacitors also being contributing factor to reducing noise. By reducing the *loop area* between the power pins and ground pins, noise can be reduced. Large loop areas during the presence of high pulsed currents give rise to noise and radiated emissions [Katrai and Arcus 1998]. Using the SO-24 surface mount package means that decoupling can be placed close to the package with minimum loop area. This is a problem associated with DIP packages where the power supply and digital supply are on opposite corners making the layout more difficult for high frequency design [Atmel Corporation 2010].

An external pull-up resistor and grounded capacitor on the reset pin ensures that the MCU can not reset inadvertently during operation.

4.2.1.1 Pulse Generator and Control board interface

Signaling between the control board and full-bridge boards are susceptible to ringing due to long tracks and large loop area. As shown in Figure 4.3, the interface between the control board and full-bridge boards consisted of 16-pin headers connected through ribbon cable via latches. To reduce cross-talk between adjacent signals in the ribbon cable alternating ground wires were used between signals.

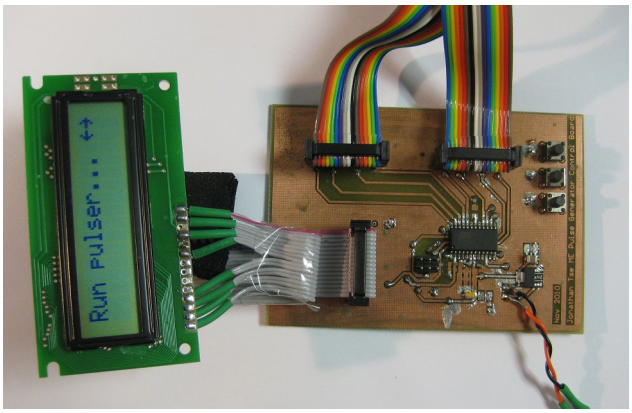


Figure 4.3 Digital Control Board including interface cabling and LCD interface.

4.2.2 Pulse Generation

The output states to the pulse generator were preformed sequentially, requiring a minimum of 19 instructions for a single bipolar waveform pulse. This is given by the number of switching states needed for a full bi-polar waveform in a cascaded configuration, and to ensure that the lower switches are turned on long enough for adequate bootstrap charge. Given this constraint, the maximum frequency realisable was 400 kHz for a cascaded two stage configuration. Figure 4.4 and Figure 4.5 show the I/O output waveforms for four consecutive pulses generated for the high voltage and low voltage stage respectively. GPIO pins are configured for driving the pulse generator. Traces 1 and 2 are high-side and low-side respectively for the left switching leg. Traces 3 and 4 are low-side and high-side respectively for the right hand switching leg. When the pulse generator is not pulsing, the low-side MOSFETs show a *normally on* state in order for the bootstrap capacitors to be charged.

The minimum amount of dead-time depends on the switching characteristics of the MOSFET. As the slew rate becomes more obvious at high frequencies, the potential for shoot through current increases. Ideally the dead-time should be chosen to be greater than the maximum switching time of the MOSFET. This strategy would be used to reduce switching losses while reducing cross conduction of switching legs. 128 ns was the minimum amount of delay achievable in a AT90PWM2B and is shown in Figure 4.6 with overlapping signal traces for a switching leg. At high-frequency, over-shoot

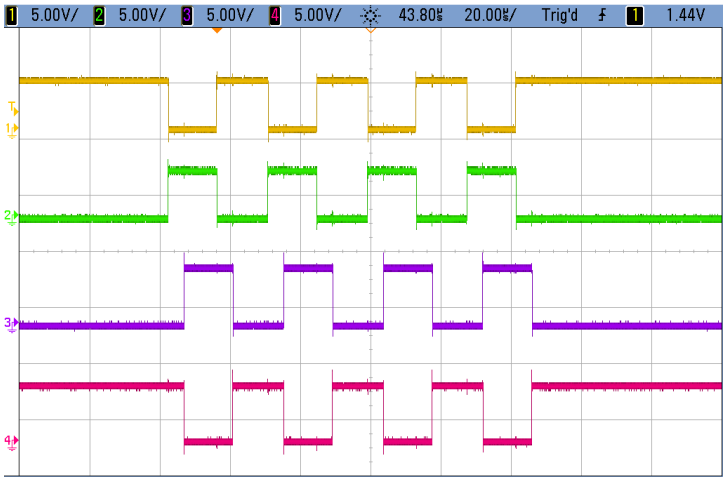


Figure 4.4 MCU output pulse waveforms for the High-voltage stage switches

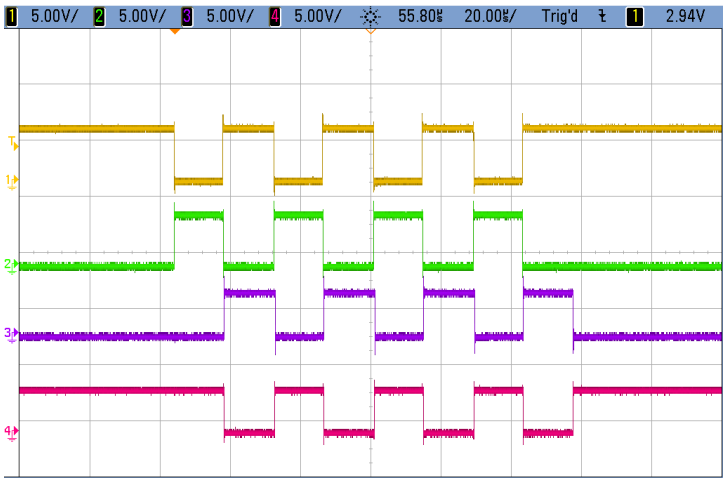


Figure 4.5 MCU output pulse waveforms for the Low-voltage stage switches

and under-shoot can be observed during turn-off and turn-on; however, this is likely to be filtered through the isolation stage.

4.2.3 Software and User Interface

The source code for the AT90PWM2B was written in C as it could be easily debugged. Use of assembly functions was also made for the small timing requirements. In particular, no operation (NOP) instructions were used for delays of 64 ns.

The main tasks of the MCU are to receive user input and generate timing critical pulses for the fullbridge stages. As researchers will regularly use the pulse generator, it is important that it has a user friendly menu interface. For electroporation pulse configurability, the following parameters were able to be modified through the LCD and button interface from the control board:

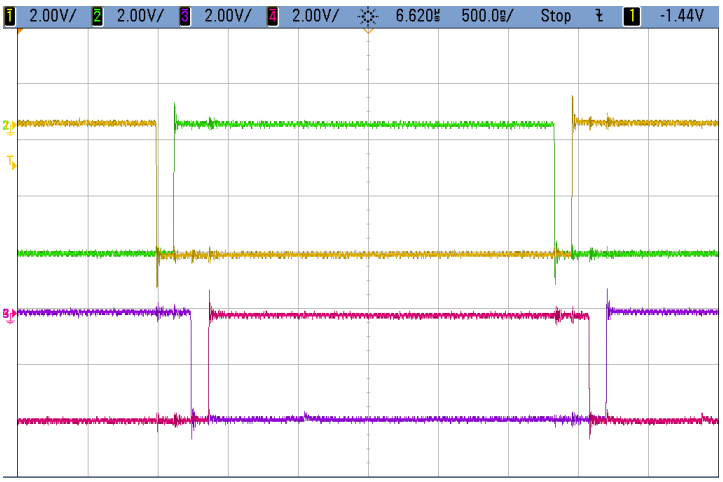


Figure 4.6 Minimum dead-time of 128 ns shown for both switching legs of the High-Voltage stage

- Frequency of pulses (default 100 kHz)
- Number of consecutive pulses (default 10)
- Duration between pulse burst (default 512 μs)
- Duty cycle of the HV stage. (default 25%)

The pulse generator is first set by default at low frequency, low repetition rate and large consecutive pulse duration. This is to ensure devices are operating properly. The pulse generator is able to be stopped while pulsing; this requires the MCU to run to the end of the last switching waveform instruction. Stopping the pulse generator inadvertently through a switching waveform would result a constant current through switching devices and, depending on the load, may exceed MOSFET specifications. The waveshape specifications (as shown in Chapter 1) inherently calls for the low voltage stage to be at a 50% duty cycle. Dead-time was set at the minimum switching period of the MCU - 128 ns. As the period between deadtime requires two operations (compare and configure output), it requires a two clock cycles (2×64 ns).

4.2.4 Code Summary

Shown in Figure 4.7 is a flow chart of the MCU during operation. GPIO pins are configured as outputs with internal pullup resistor set. During start up it is assumed that the pulse generator may have a switch turned on, the initial states for the H-bridge are therefore forced off. This limits the chance of a short circuit. For periodic pulsing and continuous pulsing, the lower MOSFETs of each switching leg are required to be turned on so that the high-side bootstrapping capacitors are fully charged. As symmetrical bi-polar waveforms were required, two integer variables were used to store the on-time and off-time referred to the high-voltage stage shown in Figure 4.8. These

timing variables were used for both positive and negative cycles of the pulse waveform. The on-time for the low-voltage stage is given as the on-time plus the off-time as it will have a 50% duty cycle. A look up table (LUT) stored timing variables for various frequencies.

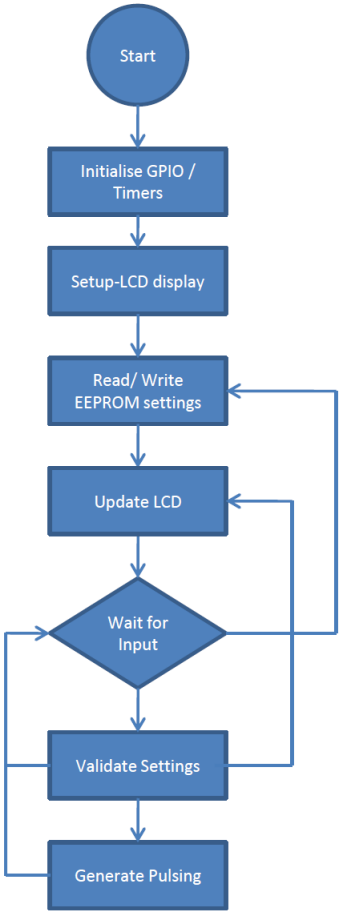


Figure 4.7 Flow chart of the controller operation

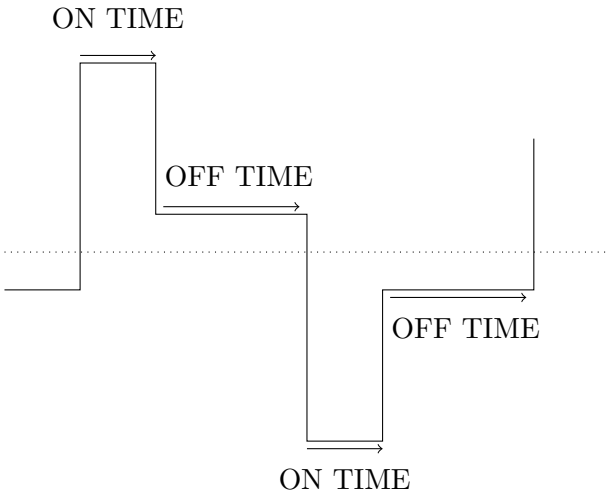


Figure 4.8 Timing variables used in the software for the MCU control board

4.3 ELECTRICAL ISOLATION AND LEVEL SHIFT DESIGN

Isolation is required between high-voltage components and digital signals. Opto-couplers provide excellent blocking capabilities where different common referenced ground nodes are needed. During full-bridge operation, the source node of the high-side circuit rises and falls from close to the rail to rail voltage of the high voltage supply.

The opto-coupler used for the pulse generator was the Fairchild HCPL-0600 (Appendix C). It is a TTL compatible opto-coupler with a listed speed of 10 MBit/s and is suitable for operating at high frequencies. The LED consists of a GaAsP LED for reliable operation. Its listed common mode rejection ratio is 10 kV/μs with a maximum output sinking current of 13 mA. The delay time between a input and output signal is listed at 45 ns for both high and low output levels. Output rise time is listed as 50 ns. The fall time is significantly smaller at 12 ns. This timing variation is expected for the BJT within the opto-device as it is not designed with high current in mind.

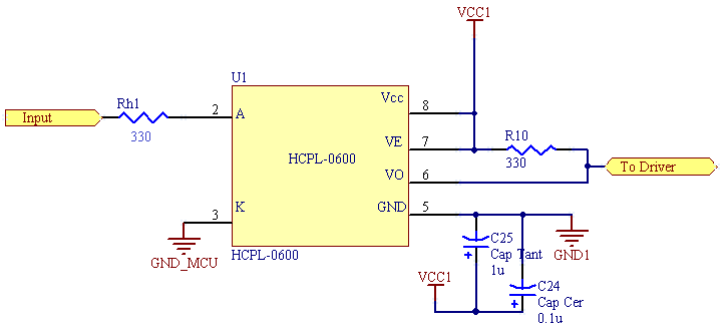


Figure 4.9 HCLP-0600 opto-coupler used for isolation and level shift. Note: V_E is not a output emitter connection, which does not exist for the HCPL-0600.

The input to the LED was current limited with a calculated 150 Ω resistor to provide a recommended 6.3 mA, for a forward voltage drop of ∼1.75 V as shown in Figure 4.9. This provides 20% current transfer ratio (CTR) degradation. The open-collector output is pulled high with a 330 Ω resistor, this provides sufficient current drive to the MOSFET driver. As a result, the output logic of the opto-coupler is inverted from the input. It is not possable to connect the HCPL-0600 in a non-inverting configuration since there is no access to the emitter of the phototransistor in the opto-coupler.

0.1 μF 2200 series ceramic capacitors were used for local bypassing which give filtering capability over a large frequency range.

4.4 MOSFET DRIVER DESIGN

In order achieve the fastest switching speed, the correct driver needs to be matched with the MOSFET. The speed at which the MOSFET is turned on is determined by how fast the gate capacitance is charged and discharged. The National Semiconductor LM5104 half-bridge driver IC was used for a lower voltage prototype stage. While it had a relatively low peak output current capability of 1.7 A (sourcing and sinking), it provided dead-time and bootstrapping on a single IC. For the high-voltage stage, the Microchip TC4422 was used as it provided a very high output current. For high-frequency switching of high-voltage MOSFETS, high peak gate current capability is required. High-voltage MOSFETs have a much larger gate charge due to Miller effect as well as the physical geometry of the MOSFET package.

4.4.1 LM5104 Half-Bridge driver for low-voltage prototype

The LM5104 IC provides high-side and low-side driver outputs through the use of *boot-strapping*. Dead-time is handled on chip through adaptive shoot through protection where the high-side MOSFET is switched according to the state of the low-side MOSFET. Through the use of a external timing resistor, the dead-time can be varied from 90-200 ns.

A boot-strapping diode, contained within the LM5104 IC, has a reverse blocking voltage range rated to 118V; therefore, the driver has a maximum output switching voltage of 103V, assuming a supply voltage of 15V. As the bootstrap diode is integral to the LM5104 IC, specific electrical parameters of the bootstrap circuit were not listed on the data sheet. Using equation 3.4, for a ΔV of 100 mV across the bootstrap capacitor, and 85 nC gate charge required for a SUP32N20 MOSFET, the estimated bootstrap capacitor size is 850 nF. 1μF was therefore chosen, these were placed externally and close the IC as to reduce loop area of high peak currents that can cause switching noise. Timing resistors of 10 kΩ were used to provide the minimum dead-time of 90 ns as shown in Figure 4.10.

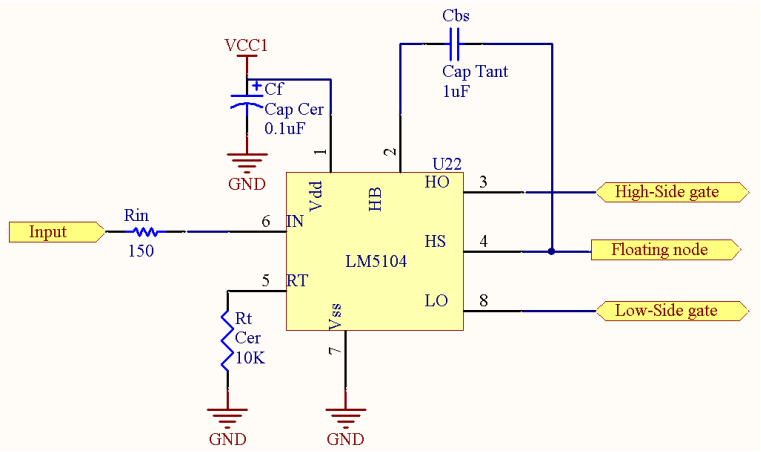


Figure 4.10 LM5104 Half-Bridge MOSFET driver with boot-strap capacitor, dead-time resistor and filtering capacitor

The LM5014 requires a single driving control signal. MOSFET switches can not independently be controlled. Outputs via HO and LO pins are complementary to one other (including dead-time); therefore, it is suitable only for a single stage design or a low voltage stage design.

For the full-bridge design using the LM5014, only two driving signals are required: a pulse signal corresponding to the output waveform and the corresponding inverting signal. The LM5104 half-bridge driver for the low-voltage stage was used in conjunction with a ATmega8 MCU, HCLP-0600 opto-couplers and logic circuitry for generating the inverting signal.

The first prototype for low-voltage stage was rated for 200 V_{pp} switching using Vishay SUP32N20 N-channel MOSFETs. The SUP32N20 MOSFETs were readily available in the electrical engineering department. They have a low R_{ds} ON of less than 0.06 Ω with a maximum pulse drain current of 80 A. Input capacitance is listed as 3100 pF; therefore, a pulsed gate current of 344 mA is expected with a turn on time of 9 ns.

4.4.2 TC4422 MOSFET driver for high-voltage stage

To drive MOSFETs for a high voltage stage, the Microchip TC4422 IC was used as shown in Figure 4.11. The TC4422 is a single channel, non-inverting gate driver with peak output current of 10 A. This is a limiting factor as to how fast the MOSFET gate capacitance can charged and discharged. Propagation delay for the TC4422 is typically 42 ns while driving 10,000 pF loads. It is able to operate up to 20V which is ideal for turning the MOSFET switch fully on with minimal on-state resistance. The rise and fall time is listed to be typically 28 and 26 ns respectively. The input is protected from disturbances through 300 mV of hysteresis [Microchip 2005]. A SOIC-8 package was selected so that optimal PCB layout could be used. The driving signal for the TC4422 was fed directly from the isolation stage with pullup resistor.

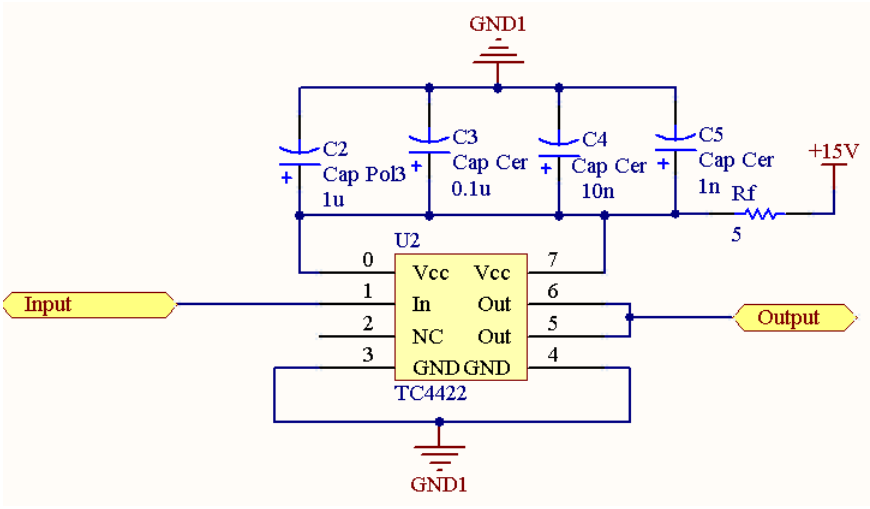


Figure 4.11 Microchip TC4422 MOSFET driver used for the high-voltage stage of the pulse generator

To mitigate noise due to high current path of the gate-source capacitance, local by-passing of the driver consisted of ceramic 3216 series capacitors. In order to filter a wide frequency range, decade steps of capacitor sizes were used: 1000 pF, 10 nF, 100 nF, 1 uF and 10 uF.

To further filter high frequency noise between voltage supplies and gate drivers, a 5 Ω resistor was used in series with the supply voltage of the gate driver. This has an effect as low pass filter with a cut-off frequency of 318 kHz. There is small voltage drop across the resistor; therefore, less voltage will be available for gate drive. At low frequencies less gate supply power is used; therefore, the voltage drop across the supply resistor is small.

4.4.2.1 Boot-strapping for the TC4422

The TC4422 is a low-side driver and therefore external circuitry is required for high side capability. The boot-strapping method for the high-side level shift was used as it is reliable and simple to design. A STTH112 1200 V rated diode was used to block the full voltage range of the high-voltage supply as shown in Figure 4.12. It has a reverse recovery time of 75 ns and a forward recovery time of 500 ns, achieving low reverse recovery losses. The forward voltage drop is listed as 1.65V, this further reduces voltage supplied to the gate drive of the high-side drivers.

The bootstrap capacitor value is calculated using equations 3.4 and 3.5. Given a ATP7F120B N-channel MOSFET, STTH12V diode, at 100 kHz, 50% duty and a on time of 25 μs the following values are used:
Q_{gate} = 80 nC
I_{LKCAP} = 3.5 μA
I_{LKGS} = 100 nA

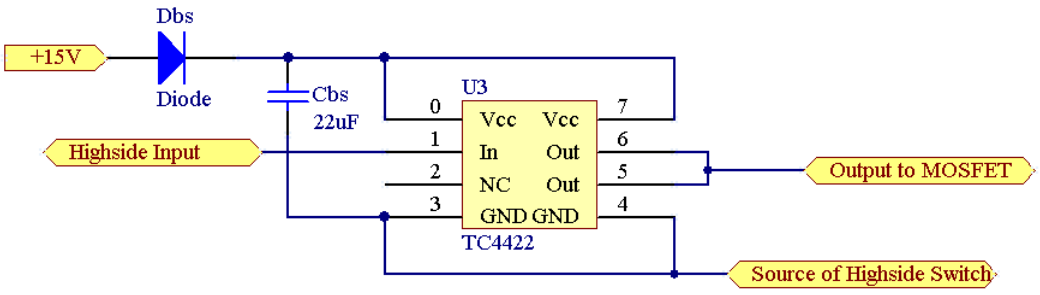


Figure 4.12 Boot strapping circuit for highside gate drive

$I_{QBS} = 120\ \mu$A
$I_{LK} = 50\ \mu$A
$I_{LKDIODE} = 5\mu$A

The total gate charge is calculated as: $Q_{TOTAL} = 83$ nC. The predominant term is the gate charge associated with the MOSFET. According to equation 3.5, at high frequency the leakage current terms become less significant. For a 10 mV voltage drop across the bootstrap capacitor, a bootstrap capacitor value of 8 μF is required. To further ensure that the bootstrap capacitor has sufficient charge for high-side switching nodes, a 22 μF tantalum capacitor in a 2917 package was used for the bootstrap capacitor. The bootstrap capacitors were rated for 35V and are somewhat protected from over-voltages of the high-side node.

4.5 FULL-BRIDGE SECTION

To achieve the fastest possible switching speeds a MOSFET was chosen which had small gate charge but high current capability. Generally high-current MOSFETs have larger input capacitances. This leads to greater power dissipation and slower switching characteristics. However, for lower current devices, dv/dt and di/dt need to be managed as the device nears the operating limits.

A useful baseline for determining switching performance is the ratio of C_{rss} and C_{iss} [Koonce 2003]. The Millar capacitance is a major problem that determines rise and fall time and it is ideal that this ratio is reduced. The ratio of the gate-source capacitance C_{gs} and C_{gd} has an effect on dv/dt [Semtech 2004].

The intrinsic body diode of the MOSFET is inherently slow and limits fast switching. It can give rise to large reverse recovery currents if parasitic inductances are not managed. An external diode is placed in parallel with the drain-source of the MOSFET and is added so to ensure that it conducts first. Shorter dead-times also reduces this effect [White 2008].

IXYS IXFH14N100Q2 MOSFETs (Appendix C) were initially used for the high-voltage full-bridge stage. These have a large input capacitance (5.1 nF) but have a large pulsed current capability of 104A. However, during testing, switching times were slow and large spikes during switching transitions were observed from a result of a high input/output capacitance ratio.

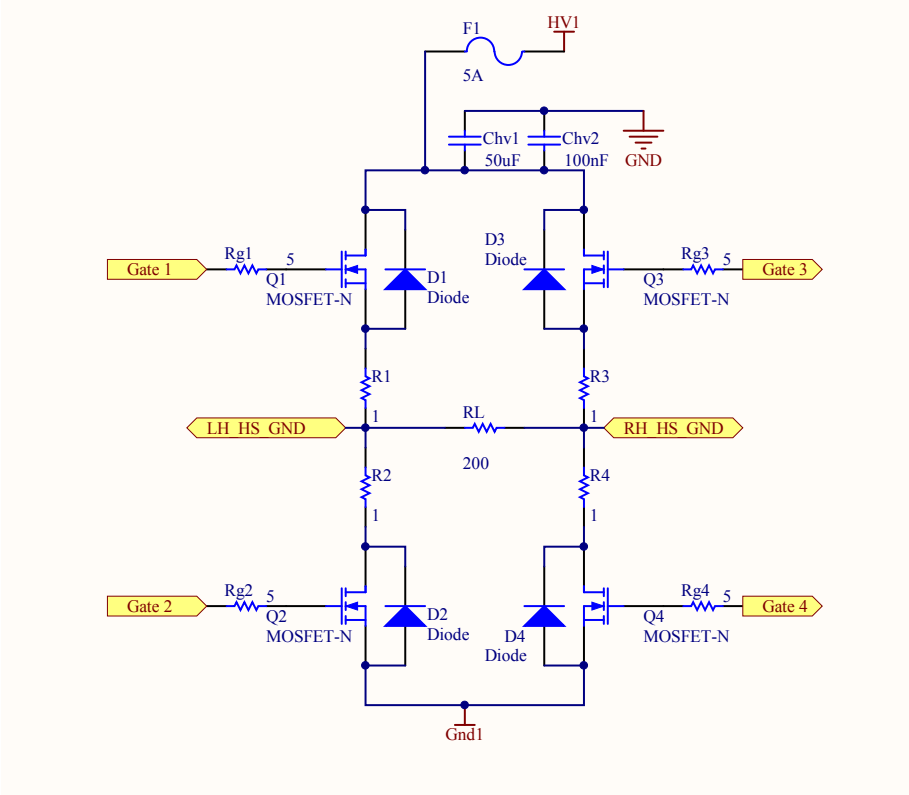


Figure 4.13 High-voltage fullbridge stage

The Microsemi ATP7F120B MOSFETs (Appendix C) were later used for the full-bridge stages. These MOSFETs provided the benefits of a high pulsed current capability of 28 A, low input capacitance of 2565 pF and a lower $C_{rss}\backslash C_{iss}$ capacitance ratio compared to the IXFH14N100Q2. The N-channel device is used in applications for zero voltage switching and are suitable for full-bridge design. These MOSFETs are ideal for a high-voltage stage, with a break-down drain-source voltage of 1200 V. The continuous drain current at 25 °C is listed as 7 A, limited by a maximum junction temperature. As expected for high-voltage MOSFETs, the $R_{DS(on)}$ is quite high and is listed as 2.90 Ω.

The peak output current required to drive the gate is calculated through equation 3.6. Given a V_{ds} switching voltage of 600 V, with a V_{gs} voltage of 10 V, with a total gate charge of 80 nC and a desired transition time of 20 ns, the required peak output current is 4 A. The TC4422 is sufficient for operating the MOSFET under those conditions. In an attempt to prevent excessive dv/dt, an external 5 Ω 2020 series gating resistor was

used.

IXYS DSEI12 diodes, in TO-220 packages, were used for the external body diodes. These have a small reverse recovery time of 50 ns with a reverse blocking voltage of 1.2 kV.

Power dissipation of the MOSFET driver is also determined from the gate charge. Using equation 3.3 the gate-driver is required to dissipate 0.24 W at 200 kHz. At 1 MHz the requirement is 1.2 W.

High-voltage power supply filtering consisted of using high-voltage aluminum electrolytic capacitors to reduce voltage ripple from large current changes. The equilavant series resistance (ESR) is listed as 1.6 Ω. As the ESR is proportional to the voltage ripple on the capacitor bank, a 24 V voltage ripple is expected for a 5 A pulsed current load. However this will be negligible during high-voltage operation over 500 V as it is proportionally small. Three readily available 450 V rated 150 μF electrolytic capacitors were used in series. Parallel placed 100 nF 2 kV rated ceramic capacitors were also used to bypass high-frequency noise to ground.

4.5.1 Low-Voltage Isolated Supplies

Floating desktop power supplies were used to power the opto-couplers and gate-drivers in conjunction with bootstrapping as shown in Figure 4.14. The setup for the power supplies is shown in the following Chapter.

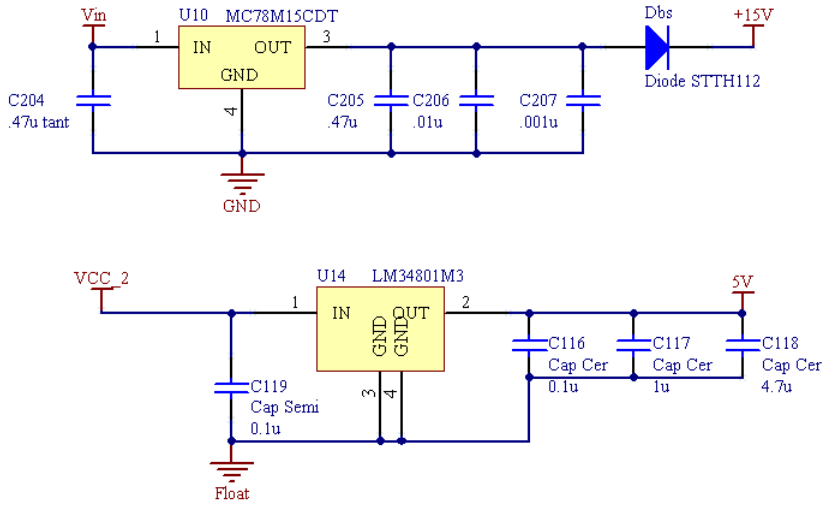


Figure 4.14 15 V Power supply regulation for gate-drivers and 5 V supplies for optocoupler outputs

4.5.1.1 5V supply for digital logic

Opto-couplers were powered with LM34801M3 low-dropout 5 V linear voltage regulator, providing maximum current output of 100 mA. Local by-passing consisted of 0.1 μF

ceramic capacitors on the input and output pins. Separate regulators were used for each high-side node of the pulse generator as they are have independent floating reference points. Since the low-side switches operate on the same reference ground, a single regulator was used for both low side switches. This made layout with high frequency considerations easier to achieve.

4.5.1.2 15V supply for gate driver

The power supply for the gate-driver circuitry consisted of 15 V MC78M15 linear voltage regulators with maximum output current of 500 mA. A 15 V output was chosen so the MOSFET is fully turned on during switching. Output filtering consisted of 0.47 μF tantalum capacitors.

4.6 PCB LAYOUT AND CONSTRUCTION OF THE PULSE GENERATOR

The construction of the pulse generator was carefully considered to enable fast operating frequencies while countering switching noise. The layout of components is critical for limiting noise sources and noise coupling. The main concern is parasitic inductances, which through inductive noise gives rise to voltage ringing during switching transitions. From basic principles, a 1 nH parasitic element in the circuit will cause a 1 V voltage drop across it, given a 1 A/ns current rise.

The main consideration to the gate-drive circuit and full-bridge was reducing the inductive loop area. Using a smaller loop area also reduces the impedance. As shown by Figure 4.15, the areas of high peak current during switching are illustrated [Chen 2005]. During switching, the gate drive loop has significant peak current through the input capacitance, this area is minimised to limit switching noise. The output voltage seen at the load can therefore be controlled more reliably. The load current also has significant current rise, this is associated with MOSFET output capacitance, power supply parasitic components, and ground. For high current loads, oscillations will occur on the output load. Ground loops also exist for multiple connections to ground. Varying impedance paths to ground will have components at slightly different potentials. Therefore, low impedance, non-looping ground paths are desirable.

The detailed PCB layout for the low-voltage pulse and high voltage stage are listed in appendix B.

4.6.1 Low-Voltage full-bridge stage construction overview

The low voltage stage was designed and tested to assess the H-bridge configuration in cascaded form. As individual switches could not be separately controlled it was deemed unusable for use in a cascaded configuration, owing to the use of half-bridge

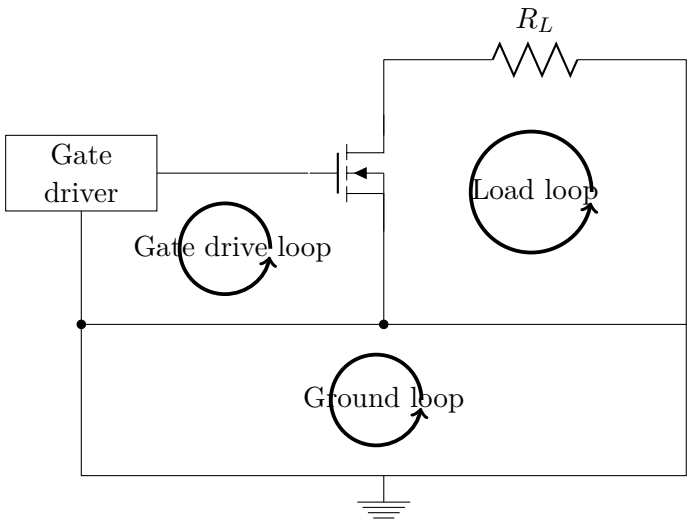


Figure 4.15 Potential high current loops associated with high-voltage MOSFET switching

drivers. PCB layout was also not as carefully considered compared to the high-voltage stage. Spare copper tracks for further additions was not considered and made further improvements difficult. Bulk decoupling for the high-voltage power supply was one area not carefully considered. Adding further decoupling capacitors would be difficult, additionally to making testing difficult. It was also not practical to have synchronous control signals going to and from separate PCB board given a cascaded configuration.

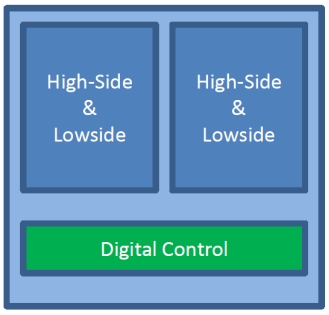
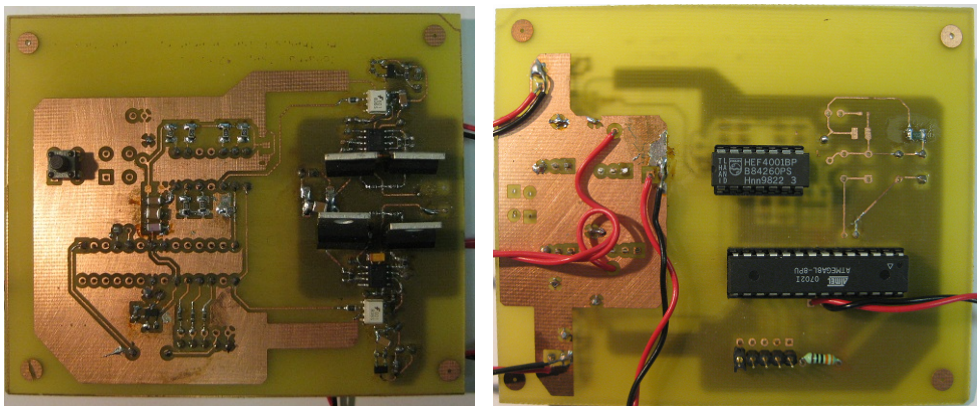


Figure 4.16 Low Voltage stage PCB layout layout scheme

A single PCB design was used, as shown in 4.16 and 4.17. This provided an all in one pulse generation solution. The PCB was separated into sections of digital logic and high-voltage switching section. The advantage of such a layout is that short traces can be made between the MCU and gate drive.

Creepage was deemed not to be be an issue at low switching voltages; therefore, TO-220 packages were used. As LM5104 is a half-bridge driver IC, MOSFET gate to driver output distance was difficult to minimise.

The wiring supply scheme for the low-voltage stage power supplies was not well implemented, separate leads were required for individual gate drives and optocouplers.



(a) Low-Voltage stage top layer (b) Low-Voltage stage bottom layer

Figure 4.17 Low-Voltage stage PCB

This potentially increases source inductance of components leading to higher noise sources on the pulse generator. The excess number of leads will also give rise to larger ground loops.

4.6.2 High-Voltage full-bridge stage construction overview

More considerations were undertaken on the high-voltage stage design with regards to limiting switching noise. Sharp corners on routing tracks and layers were avoided, as this gives rise to high electric field areas. The layout was kept symmetrical to maintain equal propagation delays as shown in Figure 4.18.

Sufficient creepage between high voltage conducting paths are needed to avoid flash-overs or arcing which can damage components. Generally, for 1000 VDC voltages on FR4 PCB substrate, a minimum distance of 5 mm is required. High-voltage supply tracks, high-side floating nodes and the low-side drain require this creepage distance. As shown in Figure 4.19, each H-bridge was built on separate boards. To reduce noise radiating to other sections, components were grouped in separate areas of high voltage and digital control. Each stage could be tested separately. Additionally, further improvements of the control board could be made.

Surface mount components were used as they exhibit lower inductance and resistance terminal connections, ideal for high frequency operation. For TO-247 MOSFET packages, 5 mm distance between drain and source terminals maintains the minimum creepage constraint. Additionally greater power dissipation can be achieved through heatsinks on TO-247 packages.

In order to reduce the amount of parasitic inductances and impedance between components, the length of routing traces were kept to a minimum. In particular, Figure 4.20 shows opto-coupler, gate drive, and MOSFET routing traces. A minimal length of 3 mm was designed between the MOSFET driver and gate terminal to reduce

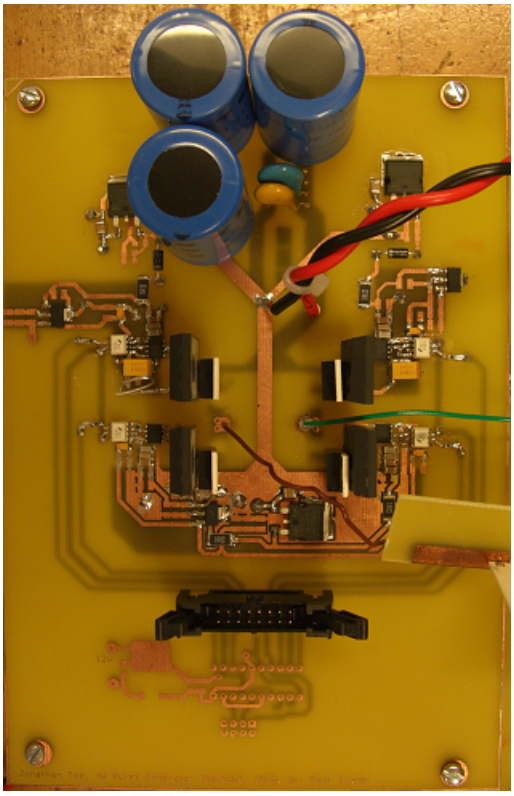


Figure 4.18 Final layout and construction of the high-voltage stage PCB

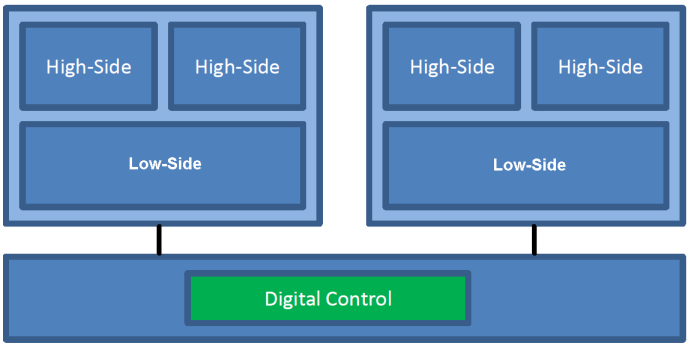


Figure 4.19 PCB layout scheme for a two stage cascaded configuration

parasitic inductance and resistance. Using the SOIC-8 package enabled the driver to be located physically close to the MOSFET gate. The length between opto-couplers and gate driver was also kept as small as possible.

Local bypassing capacitors for the TC4422 driver were placed parallel to the ground/power pins and as close to the IC as possible to reduce loop area (Figure 4.21). The lowest valued capacitors placed closest to the IC as they have a greater effect on higher frequency noise.

The loop area between gate and source of the MOSFET switches was kept to a small area. As shown in Figure 4.22, the high-side switch feedback path consists of a

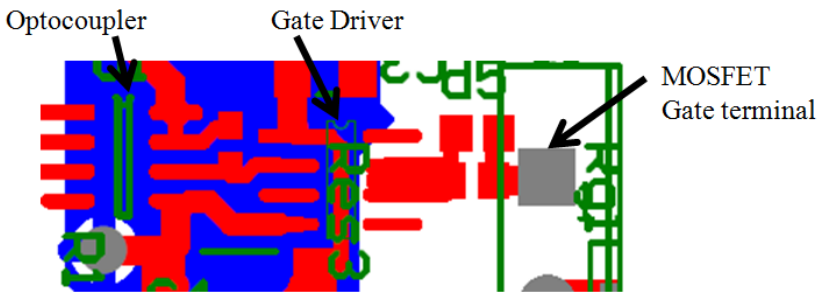


Figure 4.20 Layout of the optocoupler, gate drive and MOSFET

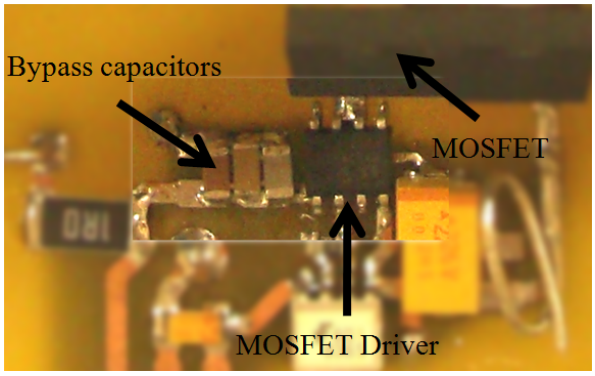


Figure 4.21 Local bypass capacitors on the TC4422

60 mil track fed directly to the ground of the gate-driver.

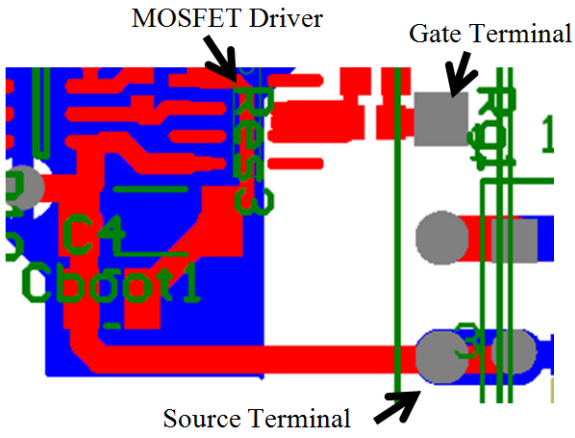


Figure 4.22 Loop area of gate-drive and MOSFET gate-source of highside switch

A symmetrical layout of the full-bridge MOSFETs and parallel diodes was used, as shown in Figure 4.23. The distance between MOSFETs, for each leg of the fullbridge, was kept as short as possible to reduce source inductance. A large gap between the bridge legs was required so that thick-film resistive loads could be placed symmetrically on the PCB. This is the optimal layout for a full-bridge configuration. High-voltage

power supply traces could then be routed under the load components giving sufficient creepage distance. For the cascaded design, the load resistors were later changed to a pair of bridging wires to connect full-bridge stages.

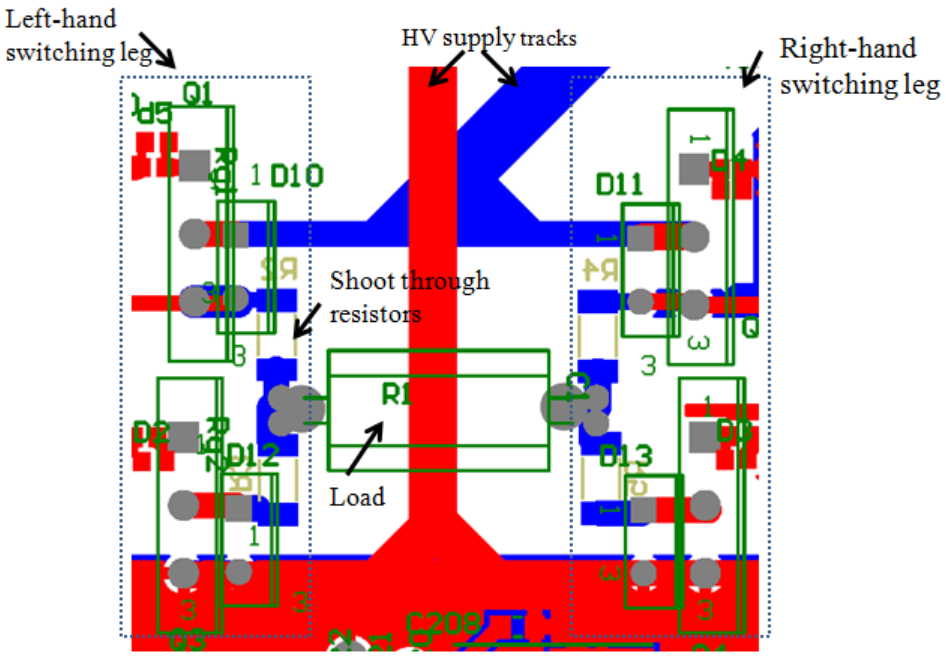


Figure 4.23 Layout of the full-bridge MOSFETs, flyback diodes, current limiting, load components.

Ground planes were used on the bottom side of each reference node for low impedance short circuit of AC noise components (as shown in Figure 4.24). A single ground plane was used for both low-side switches as they operate on the same reference voltage.

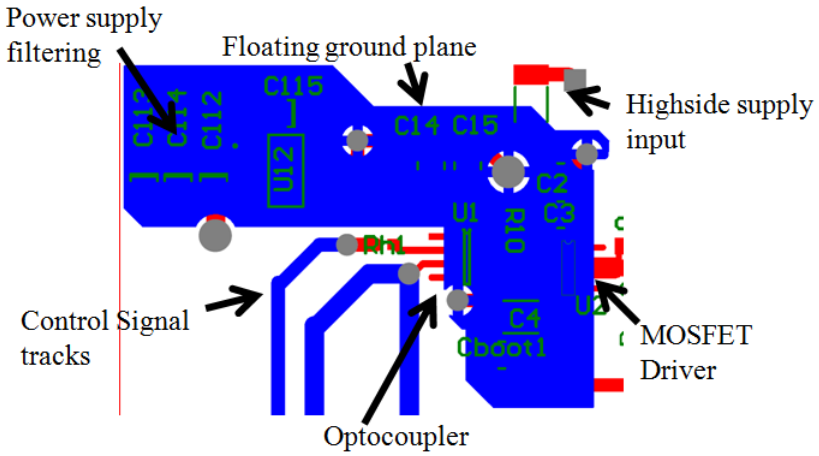


Figure 4.24 Ground plane for high-side node (bottom layer)

The high-voltage supply tracks, supplying the full-bridge MOSFETs, were the longest. These were unavoidable since high-voltage positive and high-voltage negative are located on opposites sides of the full-bridge design. The physical size of the

high-voltage bulk decoupling capacitors were large. Therefore, it was not possible to completely minimise the length of high-voltage traces. As in Figure 4.25, wide 120 mil power and ground high-voltage traces were used to reduce impedance.

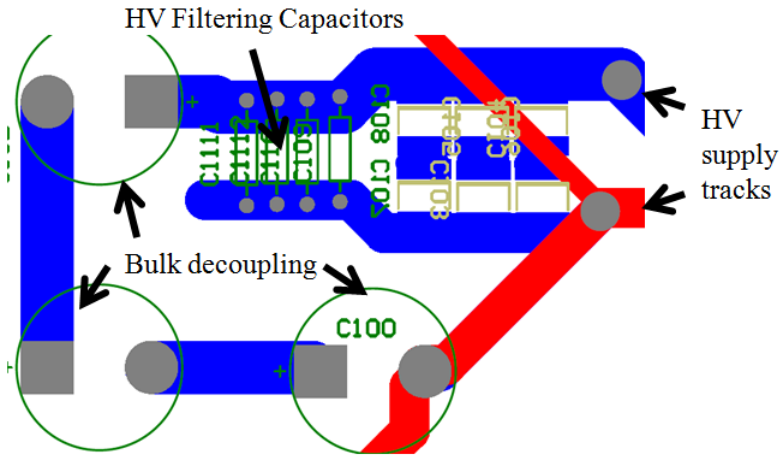


Figure 4.25 Layout of the high-voltage decoupling capacitors on the pulse generator

The current limiting resistors R3, R4, R5, R6, were placed on the bottom layer to free up space on the top layer but also to provide room for load resistance and capacitance (Figure 4.26).

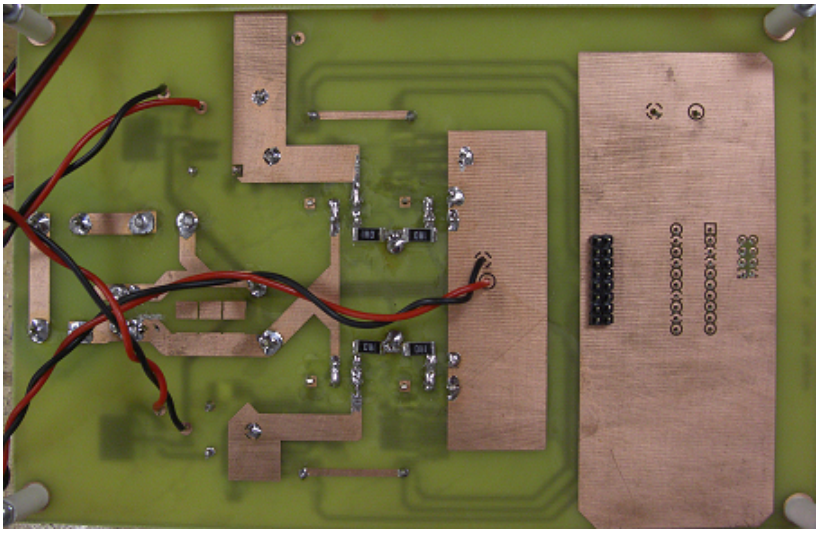


Figure 4.26 Bottom layer of a high-voltage stage showing: ground planes, current limiting resistors and low-voltage power leads

External to the circuit, fast-blow fuses were added to the high-voltage supply leads. This served to protect the MOSFET switches from excessive current. Short circuit could occur during a false gate signal or incorrect gate control during development. However, compared to the potential switching times of the MOSFETS, the time at which the fast-blow fuse reacts is significantly large and therefore will not serve for any

protection against small shoot-through current.

4.7 SUMMARY

A signal control board was designed and built using a AT90PWM2B MCU. Output profiles of up to 400 kHz could be produced for a cascaded configuration. A minimum dead-time of 128 ns was achievable, owing to the clock limitations of the MCU. A LCD display and button interface were successfully implemented. The MCU software was written and modified throughout all stage of testing.

A low-voltage prototype stage was designed and built based upon using the LM5104 IC and SUP32N20 MOSFETs. As the LM5104 is a half-bridge driver IC, individual switches could not be controlled independently and was a limiting factor for use in a cascaded configuration. PCB layout of the low-voltage prototype was also not as carefully considered, gate drive traces tended to be long and thin because of the physical limitations to using a half-bridge driver IC and large MOSFET packages.

The high-voltage prototype stages were designed and built with more consideration to high-voltage and high-frequency switching. Using the TC4422 MOSFET driver, PCB layout could be carefully considered with respect to minimising high-current loop areas and maintaining minimum clearances for operation at 1 kV_p. The bootstrap method was used to control the highside gate circuitry; this avoided the need for multiple power supplies or gate transformers.

Chapter 5

EXPERIMENTAL RESULTS

Chapter 4 detailed the design and construction of prototype low-voltage (LV) and high voltage (HV) inverters. It was seen in tests that the LV prototype was not well designed with high-power and high frequency considerations. Therefore, a new LV inverter was designed and built based on the HV design, as it preformed better with respect to current and switching capability. Both full-bridge stages were tested individually before they were used in a cascaded arrangement. The full-bridge driving signals for the pulse generators have been produced by a AT90PWM2B MCU (Chapter 3); a 128 ns dead-time between switching legs was used.

In this Chapter, the signal generator performance is assessed. A number of tests and modifications were undertaken to improve performance to meet the desired requirements. This included taking dv/dt measurements, identifying sources of high frequency noise and creating solutions to overcome them, measuring power supplies, and modifying the output voltage profile. These are all useful parameters in determining limitations of the pulse generator. As discussed in Chapter 3, the pulse generator performance is determined by good layout practice and the choice of components for full-bridge operation. In order to determine capabilities of the pulse generator, all aspects of the pulse generator are required to be tested.

In this Chapter, the testing methodology is shown, outlining the equipment required for taking reliable measurements. The requirements of the range of external power supplies used are identified. Various loads were used and the effect these had on the pulsed waveforms. However, primarily resistive loads were predominantly used for testing. In the later stages, basic testing of the pulse generator was performed on real liquid loads using a prototype electrode arrangement.

5.1 TESTING METHODOLOGY

Figure 5.1 and Figure 5.2 shows the pulse generator setup used for testing. A 15 V DC floating power supply was used for opto-coupler and gate drive circuits. Each stage's power supply was connected through twisted pair lines to decrease total loop area, thus

reducing parasitic inductance. The control logic board used a 9V battery supply. The pulse generator high-voltage supplies (HV PSU) were tested at various voltage levels. There was not any single supply that could provide the full voltage range of between 0 and 1 kV_p; therefore, multiple power supplies where experimented with. Three different power supplies were utilised as HV PSUs: DC 60V PSU, three-phase rectified power supply, and a PWM controlled high-voltage PSU [Information Unlimited 2011]. For the cascaded full-bridge design, at least one of the high-voltage power supplies is required to be isolated with a isolating transformer. This enabled the supply to be floated and also mitigate noise from the mains supply.

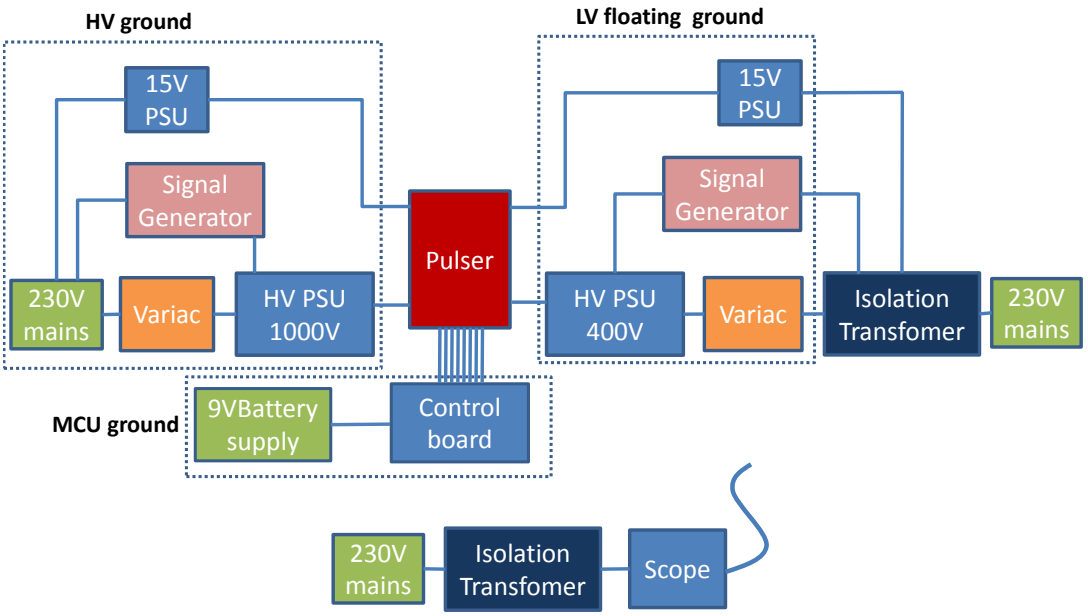


Figure 5.1 Testing setup of the pulse generator

Of the three power supplies used, only the 60V DC PSU provided adjustable current limiting ability. It was used for initial testing of the full-bridge stages. The three-phase rectified power supply provided a non-current limited 500 V DC supply with the ability to source large amount of current. Since the output is simply rectified, the voltage ripple was filtered using bulk decoupling capacitors. The voltage ripple was found to be negligible during testing. The CHARGE5000 PWM controlled PSU uses a step-up transformer. It provides low current output at high voltages of around 2 kV. A signal generator was used to set the output voltage. However, the PWM control has a limited output voltage control range. To suit the requirements of a 400 to 1000 V PSU, the CHARGE5000 was used on a variable power supply (Variac). The output capacitance is limited on the CHARGE5000; therefore, it relies heavily on the pulse generator bulk capacitors for pulse energy storage. Given that a load of 200 Ω and the bulk decoupling capacitance of 50 μF, the RC time constant is 10 ms. Therefore, only short bursts of pulses (with pulse widths of less than 5 μs) can be produced before there

is significant voltage drop from the power supply. Testing predominantly consisted of an output profile of 5 pulses at 2 Hz (as in the pulsed output profile of Figure 1.5), this gave a suitable output for assessing switching behavior and performance of the pulse generator.

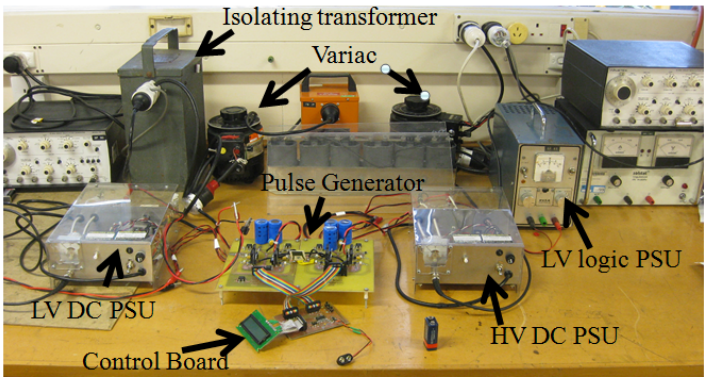


Figure 5.2 Actual testing setup in a laboratory

The main oscilloscope used was a Tectronix TDS2022B 2GS/s. Oscilloscopes were isolated using a 1:1 isolation transformer, so that measurements of floating circuitry could be measured. Oscilloscope probes consist of parallel resistors and capacitors matched to the input of the oscilloscope; therefore, it is important to reduce the loop area between the probe and grounding connection so that noise measured is not the result of probe noise.

5.2 LV PROTOTYPE TESTING

The prototype stage was tested using a 5 kΩ thick film resistor load which has a low inductance, and a power rating of 5 W. Figure 5.3 shows the output waveform for the given load on a single switching leg. The frequency set from the MCU was 100 kHz, with a duty cycle of 50%.

Large overshoot and ringing is observed during turn on and turn off of the MOSFETs. This was mainly due to poor grounding connections from the power supply to the pulse generator PCB. The high-impedance path to ground cause significant ringing and overshoot. The absence of adequate high-voltage decoupling for the full-bridge was also considered. The high-frequency component of the noise suggested that there existed some parasitic elements.

To improve performance, the high-voltage power supply filtering capacitors were enhanced with a large 150 μF electrolytic capacitor. However, this solution was not ideal as the PCB layout could not accommodate such a large physical capacitor size.

The output frequency was reduced to 66 kHz and the bipolar waveform inspected. The load was also changed to a higher power load of 2 kΩ. At 60 V supply, the output

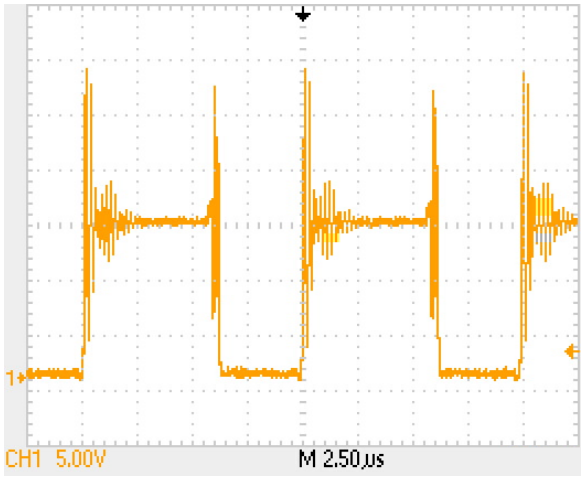
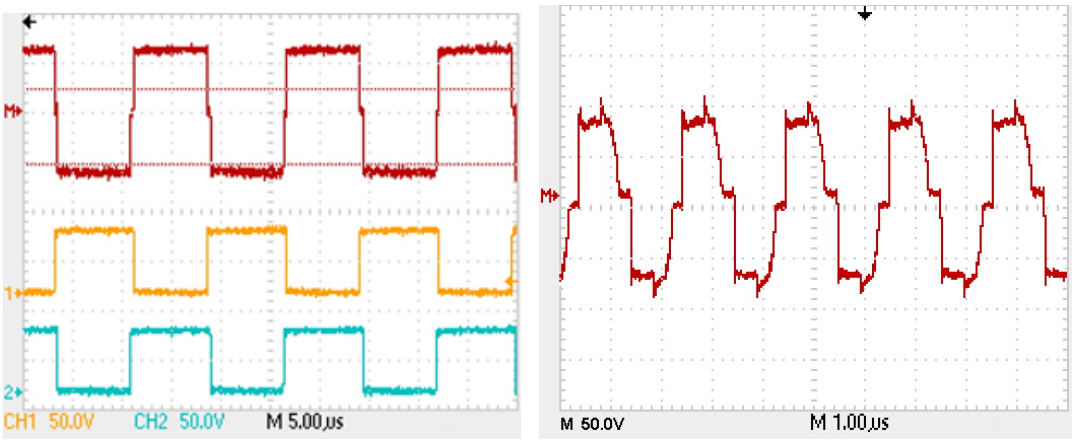


Figure 5.3 LV Stage Pulse drain-source lowside at 100 kHz

peak pulse current is 30 mA. As seen in Figure 5.4 (a), the output load waveform is seen for trace M , the peak-peak voltage is 120 V. Traces 3 and 4 are the left-hand and right hand switching legs respectively.



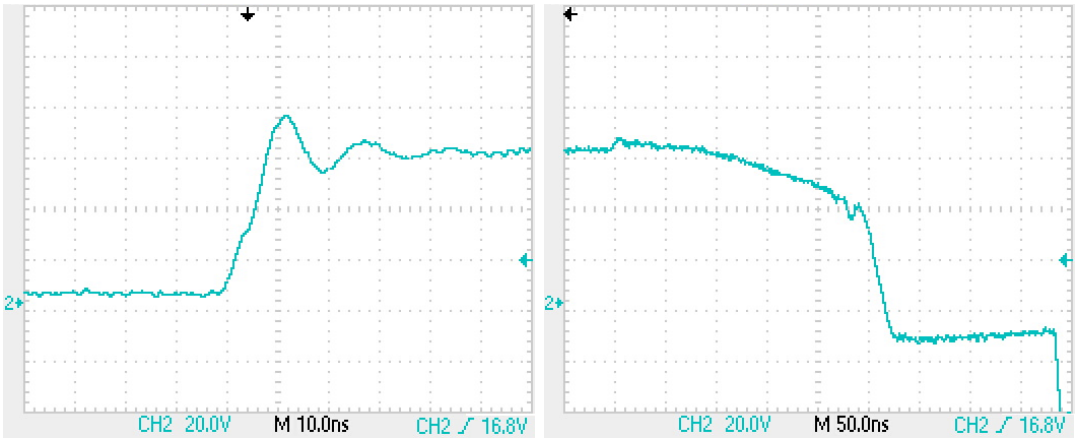
(a) (b)

Figure 5.4 Output waveform for full-bridge prototype, 50 % duty, 60 V_p (a) Bipolar output(M) and output of left/right switching legs(1,2), (b) High-frequency operation at 500 kHz

Ringing during turn-on and turn-off was no longer visible. The overshoot was also substantially reduced. A relatively sharp bipolar square wave is produced with fast rise and fall times. However, at higher pulse frequencies, high-frequency operation switching noise became an issue, even with a relatively high output resistance (2 Ω). As shown by Figure 5.4 (b), at 500 kHz, turn-on was fast, turn-off was noticeably slower.

Figure 5.5 shows close up waveforms of the rise and fall times measured at the output for the 2 kΩ resistance. A dv/dt of 6 V/ns was measured for turn-on and 0.1 V/ns was measured for turn off. The significantly larger turn off-time (compared to turn-on) suggested that the time taken to discharge the MOSFET output capacitance

was significantly large. Since a large load resistance was used, this limited i_d and hence limited the C_{ds} discharging ability of the MOSFET.



(a) (b)

Figure 5.5 LV stage output at 60 V_p at low-frequency operation, (a) rise transition, 6 V/ns, (b) fall transition, 0.1 V/ns

While fast rise and fall times are ideal for electroporation purposes, the physical layout of the LV full-bridge prototype made it difficult to implement a cascade configuration. It is clear that single stage bipolar waveforms can be produced for a LV stage. While the LV stage should carry the same load current as the HV stage, the two stages do not require the same PCB layout clearances. Therefore, a LV stage should be able to work at higher frequencies. However, when considering the possible range of applications, it is important to keep all cascaded stages similar and suitable for high-voltage switching. For this reason, a second LV inverter was built based on the design for the HV inverter and was used for the cascade configuration.

5.3 HV STAGE TESTING

Since two similarly designed HV stages were built, each stage was tested individually as a single stage before the cascaded arrangement was used. Figure 5.6 shows the output waveform from the HCLP-0600 opto-couplers showing the dead time of 128 ns between switching legs of a single stage. There was little observable noise caused by the cabling scheme from MCU to pulse generator boards; however, any likely noise will be filtered during later stages.

Given electrical switching specifications for all the switching devices and using the ATP7F120B MOSFET, the maximum frequency can be calculated using the sum of the total rise and fall times. $T_{\text{opto(on/off)}}$ is the optocoupler turn on/off time, $T_{\text{gatedriver(on/off)}}$ is the gate driver turn on/off time, $T_{\text{mosfet(on/off)}}$ is the MOSFET turn on/off time

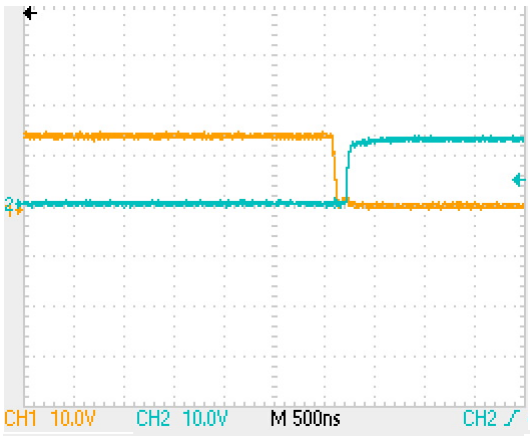


Figure 5.6 Opto-coupler output for the HV stage and dead time of 128 ns, left-hand switching leg, trace 1:highside signal, trace 2:lowside signal

For turn on:

$$T_{\text{on}} = T_{\text{opto(on)}} + T_{\text{gatedriver(on)}} + T_{\text{mosfet(on)}} = 150 \text{ ns} \tag{5.1}$$

For turn off:

$$T_{\text{off}} = T_{\text{opto(off)}} + T_{\text{gatedriver(off)}} + T_{\text{mosfet(off)}} = 145 \text{ ns} \tag{5.2}$$

From this, the theoretical maximum frequency possible is given as:

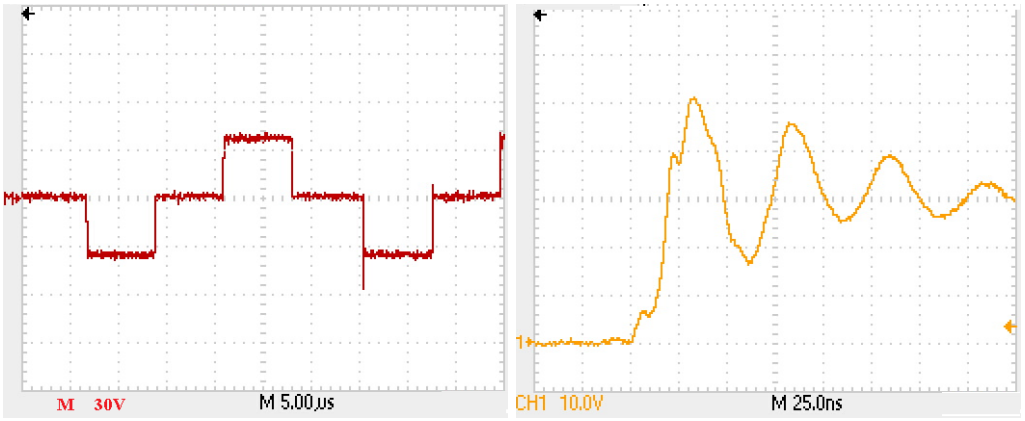
$$T_{\text{max}} = T_{\text{on}} + T_{\text{off}} = 295 \text{ ns} = 3.4 \text{ MHz} \tag{5.3}$$

Applications for the designed pulse generator will not require frequencies beyond 1 MHz. As such 3.4 MHz is beyond the maximum frequency specified for this project; switching noise is likely to be the dominant problem. Moreover, the MOSFET would spend a significant amount of the time switching and therefore, switching losses would be high.

5.3.1 HV single stage tests

A thick film resistive load of 200 Ω was used using the IXYS IXFH14N100Q2 MOSFETs for the HV stage board. The use of the smaller load resistance will result in a much higher pulsed current. A 25% duty cycle at 50 kHz was used to illustrate the switching action for a HV stage. The output was pulsed at 1 ms interverals, every 15 ms to reduce the power dissipated by the resistor. As seen in Figure 5.7, the output is virtually noise free; however, periodically during turn-on, of the left-hand switching leg, large overshoot and oscillations occur. On closer inspection, these were oscillations with a frequency of 50 MHz indicating parasitic inductance coupled with MOSFET

drain-source capacitance inducing noise on the output. The voltage spike peaks are 45% of the supply showing that stress on the MOSFET could occur at high voltages through, both for over-voltage, and excessive dv/dt.



(a) (b)

Figure 5.7 Output 30 V_p waveform for 200 Ω load at 50% duty (a) voltage waveform, (b) zoomed view of turn-on event

The use of ATP7F120B MOSFETs on the HV stage yielded less spikes observed when switching. As shown in Figure 5.8, the pulse train was modified to produce a 25% duty with a peak voltage of 600 V, at a switching frequency of 133 kHz. The high frequency noise at turn on is indicative of parasitic elements being excited due to large current changes. However, at turn off, on both positive and negative switching cycles, the high-frequency noise was absent. The parasitic elements associated with the load resistance could not further be minimised as they are located on the PCB.

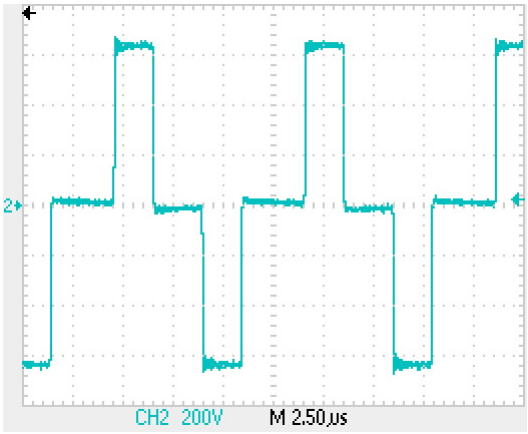


Figure 5.8 Output voltage for 200 Ω load at 600 V_p, <2.5 μs pulses

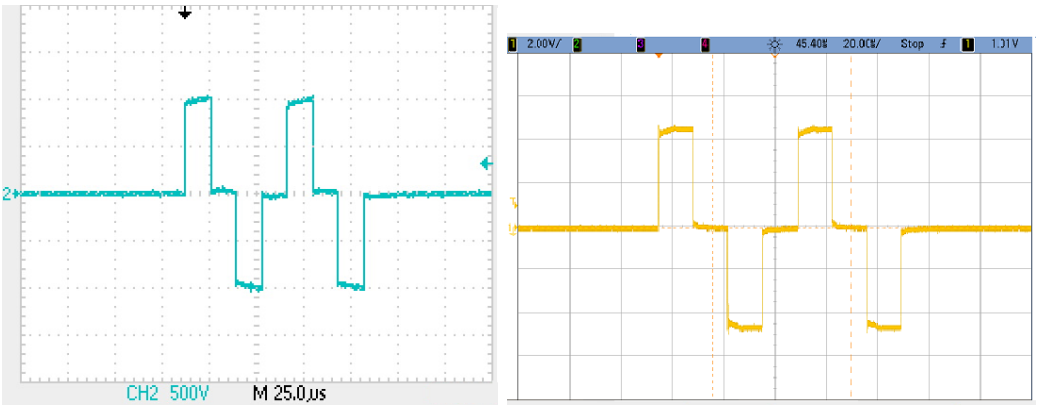
The HV stage using the ATP7F120B MOSFETs was tested up to 1 kV_p using the CHARGE5000 power supply. As potentially lethal voltages were being switched, a 100 kΩ high-power bleeding resistor was placed in parallel with the high-voltage bulk decoupling capacitors. This gave a time constant of 5 s which dissipated any capacitive

charge during non-switching periods. However, upon testing, the supply could not sustain 1 kV while connected to a 200 Ω load through the pulser.

With the bleeding resistors removed, pulsed output at 1 kV_p was sustainable from the CHARGE5000 PSU. Figure 5.9 shows the output with the corresponding current waveform with scales of 500 V/div and 2 A/div respectively. Some of the low frequency ringing was removed through shorter load leads. This reduces the loop area and hence decreasing the parasitic inductance. No other high frequency noise was visible. The peak load current was measured at 4.6 A, this indicates that a small amount of the power was being dissipated in the current limiting resistors and the MOSFETs. The expected peak output current was:

$$R_{total} = R_{mosfet} \times 2 + R_{currentlimiting} \times 2 = 208\ \Omega$$

$$1000/R_{total} = 4.8\ \text{A}$$

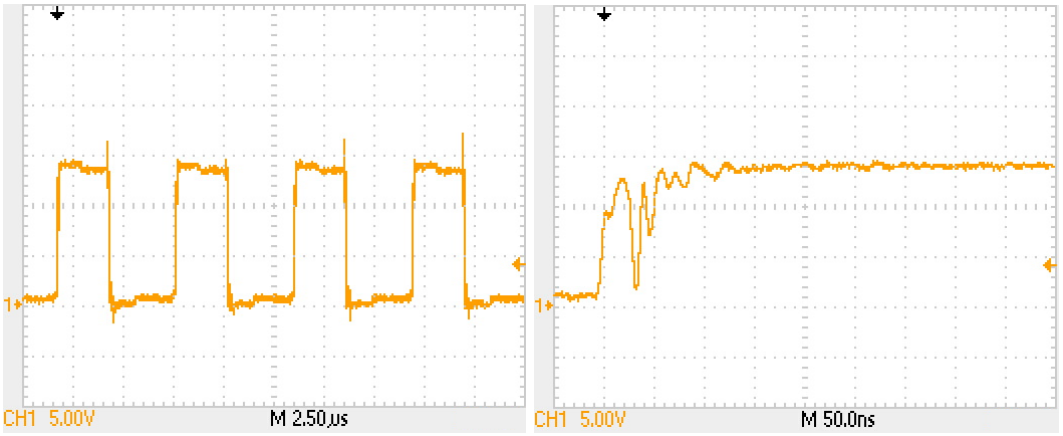


(a) (b)

Figure 5.9 1 kV_p operation at 20 kHz with a 200 Ω load, (a) voltage waveform, (b) corresponding current waveform (2A/div)

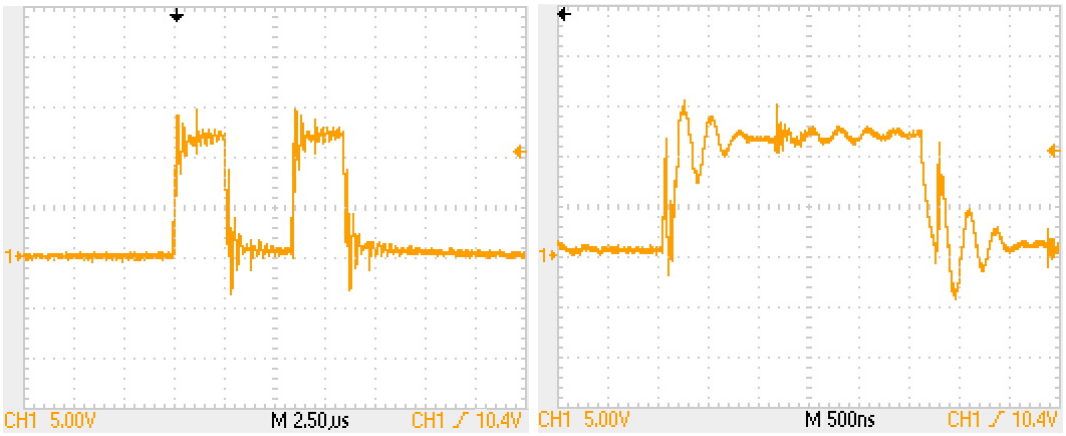
Figure 5.10 shows the lowside gating waveforms at an output voltage of 1 kV_p. It was expected that at high output voltages the gate would be more prone to noise as switching currents increase. On observation, the gating signal is relatively noise free and will not severely affect the output waveform. During turn on, the Miller effect can barely be seen. The transitions are relatively fast; less time in the active region will lead to smaller switching losses. When the MOSFET is turned on, false turn-off can be observed around 40 ns later. However, the turn-off period observed is so short in duration, and close to the turn-on event, that it has no effect on the output waveshape.

As seen from Figure 5.11, the highside gate waveform appears considerably worse, suffering from high frequency oscillations and overshoot at both turn-on and turn-off. A turn-on voltage level of 13 V was expected since there is a voltage drop of 1.65 V across the bootstrap diode for the highside MOSFETs. Most noticeable is the high frequency oscillations during turn-off. These oscillations occur outside the dead-time region and are greater than the MOSFET threshold voltage (4 V). Shoot through



(a) (b)

Figure 5.10 Lowside gate terminal waveform at 200 kHz with an output voltage of 1 kV_p, (a) lowside gate, (b) closeup view of turn on



(a) (b)

Figure 5.11 Highside gate terminal waveform at 200 kHz with an output voltage 1 kV_p, (a) highside gate for 2 pulses, (b) closeup view of high frequency oscillations

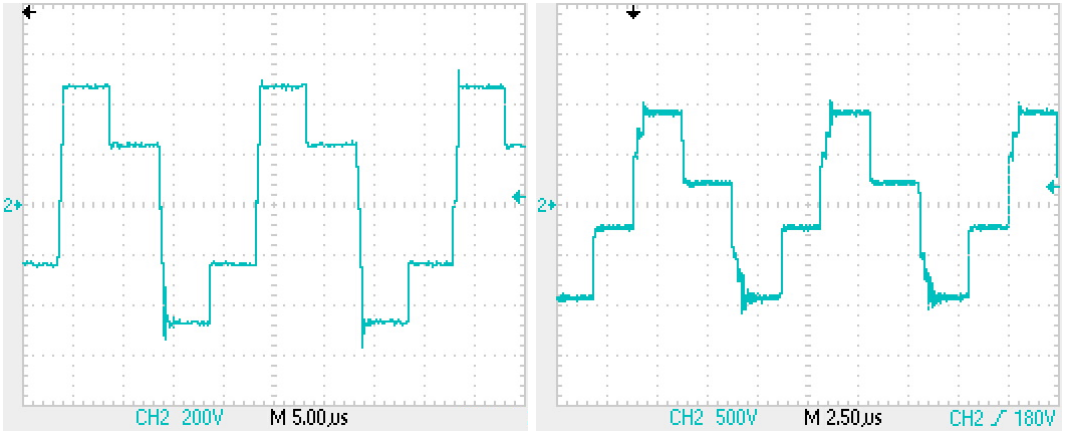
current could occur during this period. The floating highside common swings between 0 and +1000 V_p, this creates a great deal of common-mode noise that can effect the driver and MOSFET gate. Ideally the MOSFET switch should withstand a great deal of common-mode interference. When looking at the output waveform at 200 kHz, there is no observable effect of shoot-though current or high-frequency oscillations of the gate.

5.3.2 Cascaded design output results

As each H-bridge stage was designed with high frequency considerations, it was expected that cascading two stages will have increased noise on the output waveform due to an increase in the overall load loop area. The total load current loop now consists of the area between both boards and the interconnections between stages. Initial tests using a cascaded arrangement showed unstable waveforms with low frequency noise.

However, this was caused by incorrect grounding of power supplies. Using the test setup as shown by Figure 5.2, better results were observed.

Figure 5.12 shows a bipolar two-stage (5-step) output waveform. At high operating frequency, high frequency noise was observed on the rising edges of the high-voltage pulses of both negative and positive cycles.



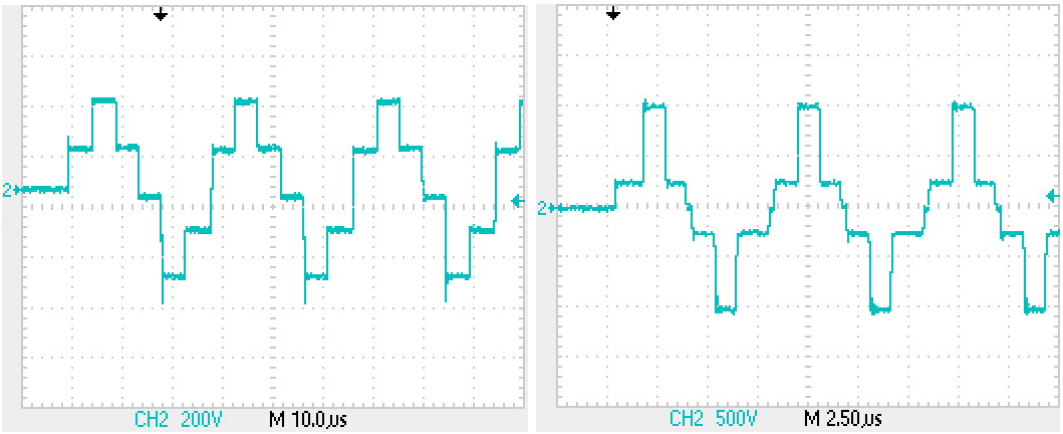
(a) (b)

Figure 5.12 200 Ω load at 50 kHz, cascaded output profile, (a) 50 kHz, 440 V_p (200 V_p LV stage, 220 V_p HV stage), (b) 100 kHz 990 V_p (240 V_p LV stage, 750 V_p HV stage)

In order to investigate the effects of the switching noise associated with the negative cycle, the duration between switching periods was changed to equal delays, as shown by Figure 5.13 (a). It was seen that on the negative cycle, the low voltage stage was not turning on. The ringing, observed during previous tests, was due HV stage switching on before the LV stage. As large currents are being switched, ringing was observed on the high-voltage pulse. The code for the MCU was modified to produce the corrected staggered square-wave output profile. As shown in Figure 5.13 (b), an output voltage level of 1 kV_p was obtained at 133 kHz. High frequency oscillations were still visible, but only during the negative rising edge of the LV stage. This lead to the assumption that the LV stage is not as symmetrically constructed. The HV stage performed somewhat better, being relatively noise free during both switching transitions. 1.5 μs, 800 V_p pulses from the HV stage were easily attainable, and higher frequencies could be used if needed.

The output profile was modified to again meet the specifications of the project as outlined in Chapter 1. As shown in Figure 5.14, the output profiles at various frequencies suitable for the application of disinfection are shown. Switching noise on the output was not an issue at low frequencies ($<$ 166 kHz). It is evident that there is increased oscillatory ringing associated with the LV stage, as observed at 238 kHz.

The maximum frequency the pulse generator was tested at was 238 kHz, this was due to the timing limitations of the MCU. It is clear from the output results of Figure 5.14 that the HV stage can be run at much higher frequencies. A pulse width of 1 μs was



(a) (b)

Figure 5.13 200 Ω load, staggered output profile at 66 kHz, (a) modified output profile 400 V_p, (b) corrected output at 2 kV_{pp} at 133 kHz

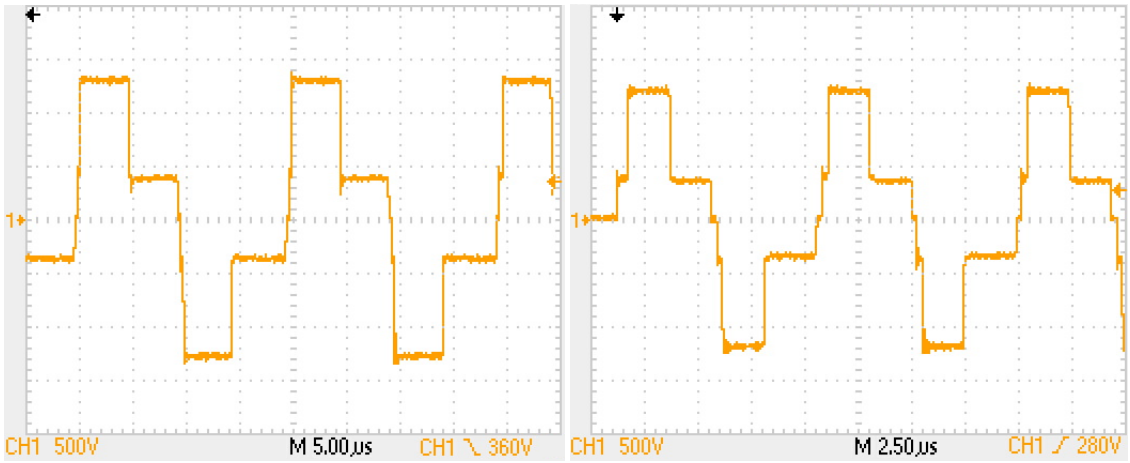
easily achievable for the HV stage. Since the HV stage comprises of the ATP7F120B MOSFETs, sharper switching transitions were seen.

Ideally, the actual switching transitions between the LV and HV stages should be as short as possible in order to maximise dv/dt for electroporation applications. Between a rise cycle of the LV stage and the rise cycle of the HV stage, a small delay is seen, this is due to the delay between instructions on the MCU. At 166 kHz and 238 kHz, this effect becomes more evident. Further development of the control board is necessary for operating at higher frequencies.

5.3.3 Output dv/dt rise and fall

The rise and fall time was measured across the load to assess limitations of the pulse generator for electroporation applications. As shown by Figure 5.15, the HV stage was measured with a rise time of 23 V/ns and fall time of 27 V/ns. The switching transitions are perfect with a switching current of approximately 6 A for a 200 Ω load. The transition is absent of noise with no over-shoot or undershoot observable. The high dv/dt observed does not appear to induce any false turn-on or turn off behavior.

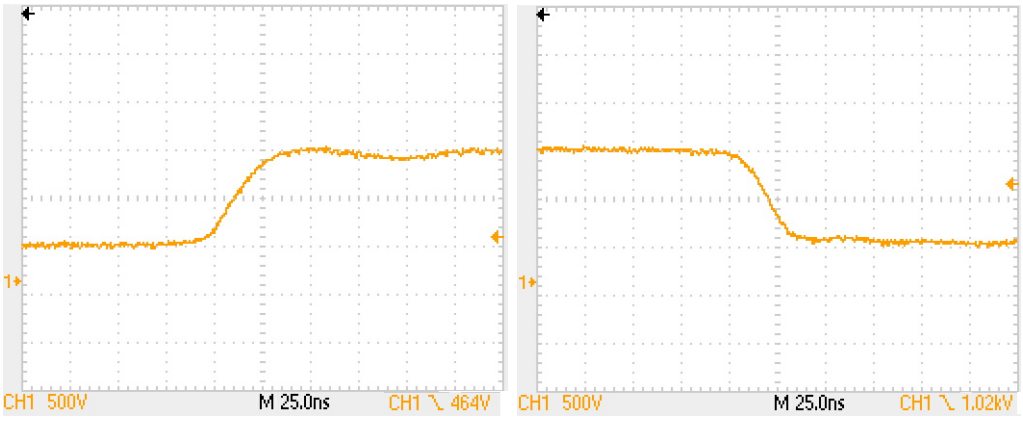
Figure 5.16 show the rise and fall times for the LV stage. A voltage rise of 20 V/ns and fall time of 6 V/ns was measured. The rise time exceeds that of the maximum dv/dt rating of the IXFH14N100Q2 MOSFETs. A higher gating resistance should be used limit the dv/dt. Slow turn-off was seen which was similar to the LV prototype turn-off. On both transitions, high-frequency oscillations was seen. Ideally an RC snubber should be employed to limit dv/dt on the output as well as to remove voltage spikes and oscillations.



(a) (b)

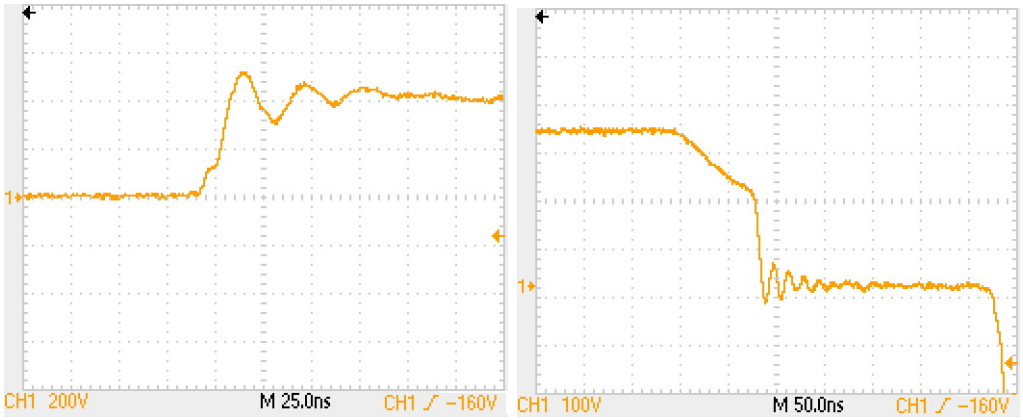
(c) (d)

Figure 5.14 200 Ω load, stepped output profile, LV stage:400 V_p, HV stage: 1 kV_p (a) 53 kHz, (b) 111 kHz, (c) 166 kHz, (d) 238 kHz



(a) (b)

Figure 5.15 Output switching transitions for 200 Ω load, 200 kHz, 1 kV_p output on the HV stage, (a) turn on, (b) turn off



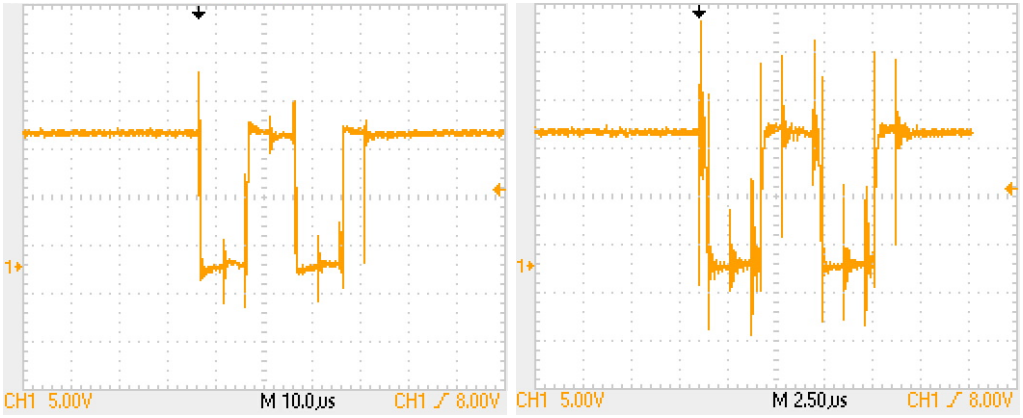
(a) (b)

Figure 5.16 Output switching transitions for 200 Ω load, 200 kHz, 400 V_p output on the LV stage, (a) turn on, (b) turn off

5.3.4 Gate signals using a cascade configuration

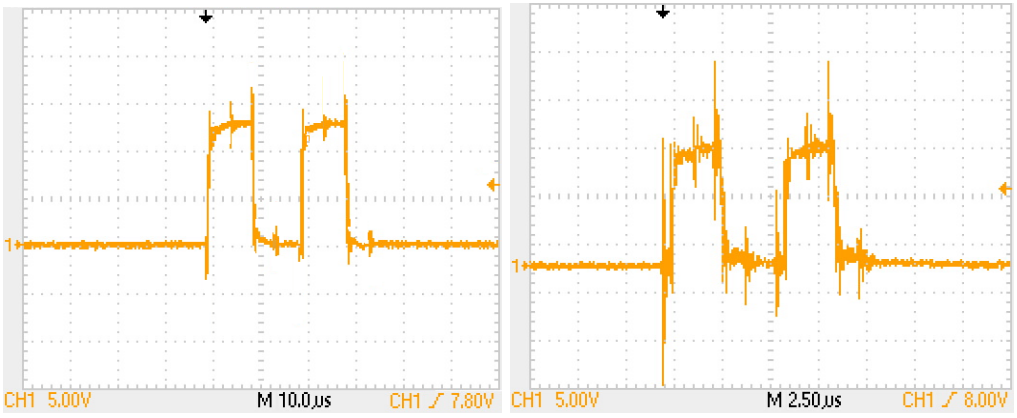
Using the cascaded configuration, significant ringing and overshoot voltages were generated on the gate terminal. It was important to take measurements directly or close to the MOSFET gate-source terminals which otherwise would give an apparent increase level of noise. Reducing the loop area between the oscilloscope probe and reference was necessary for taking reliable and accurate measurements. As seen by Figures 5.17 and 5.18, the severity of the oscillations seem to increase with increased output frequency. di/dt is expected to be consistent across different switching frequencies, therefore; the level of switching noise is expected to remain the same. However, at higher pulse frequencies, the high frequency noise simply becomes more apparent. The observed increase noise level seems to be due to a measurement artifact (hence the importance of using a suitable scope probe with minimal loop area to minimise effects of probe noise in measurements).

High-frequency oscillations also appeared to occur whenever *any* of MOSFETs are in a switching transition for the corresponding stage. The gate switching noise appears to be the result of a coupling effect from adjacent switches.



(a) (b)

Figure 5.17 Gate signal for lowside MOSFET, HV stage at 1 kV_p, (a) 50 kHz, (b) 200 kHz



(a) (b)

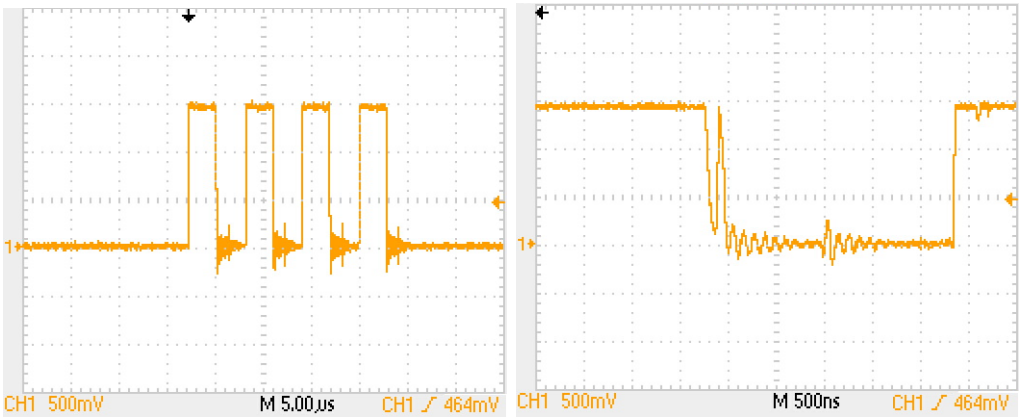
Figure 5.18 Gate signal for highside MOSFET, HV stage at 1 kV_p, (a) 50 kHz, (b) 200 kHz

As with single stage testing, the high-frequency oscillations seen from gating measurements did not have a significant effect on the output waveforms. From the gating waveforms, the threshold voltage was not exceeded by a significant amount. It is evident that there is, to some extent, high-frequency immunity from the gate to the drain-source terminals.

Further investigation into improving the gate waveform is required. Under continuous use, for the likes of disinfection purposes, the noise may result in excessive power dissipation for the driving circuitry.

5.3.5 Opto-Isolation signals

Figure 5.19 shows the apparent high-frequency noise on the opto-coupler input that appeared on both the highside and lowside signals. This is the result of a coupling effect from the pulse generator. Since the highside circuitry swings between 0 and the HV supply, this creates a common-mode transient. The HCLP-0600 opto-coupler used has a rated CMR of 10 V/ns. The output rise time-of the HV stage (27 V/ns) exceeds that of the opto-coupler CMR. It is therefore not able to withstand that amount of common mode interference.



(a) (b)

Figure 5.19 High-side opto-coupler input, (a) opto-coupler voltage, (b) closeup of high-frequency noise

Attempts were made to minimise common-mode switching noise seen at the opto-coupler by using a twisted cable pair wrapped several times around a toroid. The twisted pair cable was used on a single high-side channel from directly from the MCU to the opto-coupler. The toroid was positioned close to the noise source (opto-coupler) and current limiting resistor to act as an effective high impedance at high-frequency. However, no visible change at the MOSFET gate was seen and the previous cabling scheme was used.

5.4 LIQUID LOAD TESTING

For actual load testing on liquids, a single stage pulse generator was used on an electrode apparatus designed and built by Jonathan Bousfeid at the University of Canterbury. The full system setup is shown in appendix E. As in Figure 5.20, the system consisted of a chamber to pass liquids though a 1 × 1 mm electrode system, with a 1 mm gap. A speed controlled pump allowed circulation of liquids through the apparatus of varying flow rates. Low flow rates were used as the electrode chamber was still in development stages; leaks were prone at high flow rates. High-voltage probes could be attached directly to the electrode chamber.

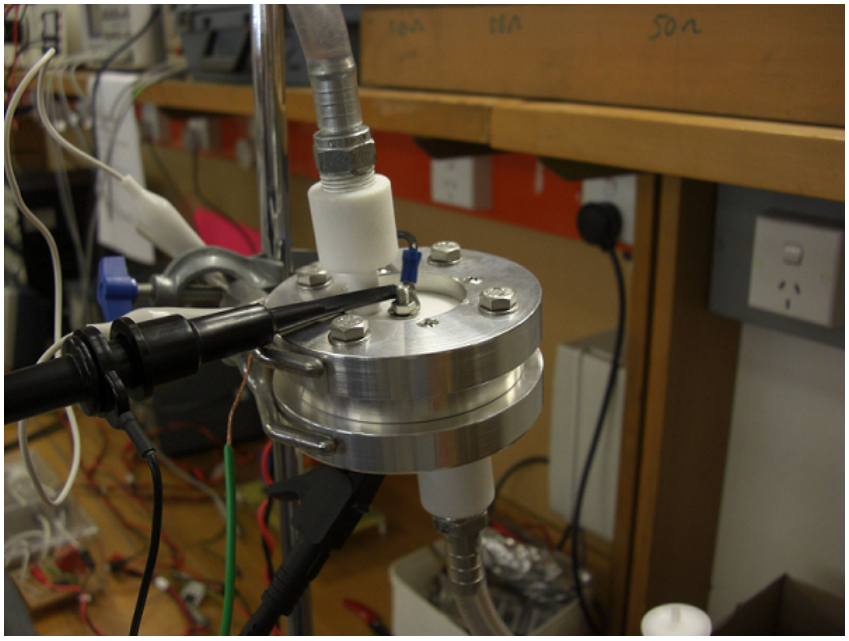


Figure 5.20 Electrode arrangement used for liquid load testing

The two testing liquids used were: Christchurch tap water and milk derived from milk power. Christchurch tap water is generally regarded high quality and would be a good representation of drinking water. The milk liquids were tested to see how the pulse generator would react to a real application.

5.4.1 Single Stage testing for actual liquid load

The inductive effect from using the long electrode leads becomes apparent when used across the electrode system. Figure 5.21 shows a voltage waveform of 520 V_p across tap water at a low flow rate. A short pulse of two bipolar waveforms were output on the electrodes at 20 kHz.

The second test involved using a very low repetition rate with 500 V_p pulses was placed on reconstituted milk measuring both the voltage and current waveform. It was originally thought that liquid foods would act as a very low resistance, drawing large amounts of current. However, it was observed from the current waveform in Figure 5.22 (b), a peak current of 2.5 A was being drawn from the pulse generator across the milk. This gave a effective impedance of $\sim$200 Ω. Large current spikes were also observed during switching transitions, this is indicative of the parasitic capacitance of the load coupled with parasitic switching components from the pulse generator. One other possible cause is shoot though current. As the load impedance was previously unknown, switching noise could be coupling to the gate and causing shoot-through currents.

Both water and milk yielded similar output voltage results as from Figure 5.21

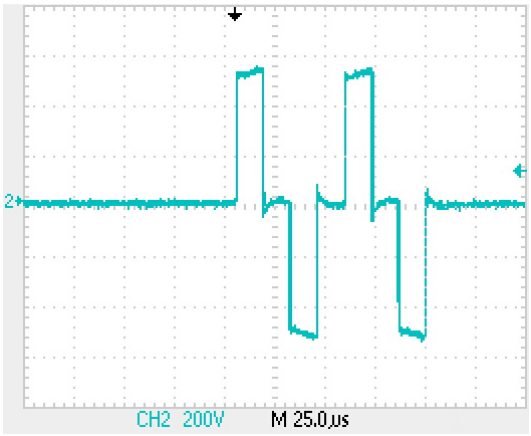
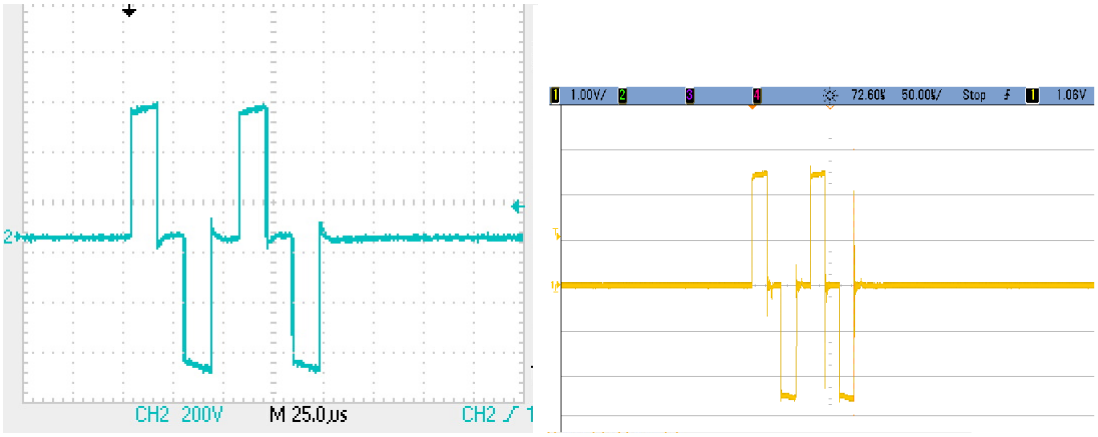


Figure 5.21 520V on Christchurch tapwater at 20 kHz



(a) (b)

Figure 5.22 Pulse generated on reconstituted milk at 520 V_p with 20 μs pulses, this waveform is ideal for the HV stage, (a) voltage waveform, (b) current waveform, 1 A/V

and 5.22 (a). During every ON state there appeared to be a charging effect associated with the power supply. The pulse width duration was significantly larger than what was previous used for tests. Unfortunately further tests were not carried out on liquid loads due to loss of resources (including time).

Chapter 6

CONCLUSION

This chapter concludes the thesis work conducted on the pulse generator. A cascaded multilevel pulse generator was successfully designed and tested. In its current state, it is capable of switching voltages of up to 1.4 kV_p at frequencies beyond 200 kHz in laboratory conditions. Full-bridge control was successfully implemented though the design and construction of a MCU board. The output frequency, pulse delay, and number of pulses could be easily be controlled through the MCU board. However, there were various limitations to the implementation which will be discussed in this Chapter.

6.1 CONCLUSION

This thesis has outlined the theory of the cascaded full-bridge design and the applications of electroporation. The H-bridge topology was described as well as semiconductor switching theory required for controlling such a design. The hardware design is presented, a prototype board was built using a LM5104 driver and two higher rated full-bridge boards were built using the TC4422 driver. For the higher rated boards, two different MOSFETs were used as the two full-bridge boards were to be used at different voltage levels (400 V_p and 1 kV_p). PCB layout and the construction of the boards was carefully considered as to limit noise sources associated from high frequency and high voltage switching. As described Section 4.6, large loop areas alongside high di/dt current can cause significant noise which were managed through design and layout. Coupling effects between the MOSFET output and drive circuitry are undesirable and can effect the output waveform. It was found that careful PCB layout is a crucial aspect for reliable operation but also allowed further developmental work. Through this, the cascaded design was demonstrated at high-voltage and high frequency, ideal for electroporation applications below 500 kHz. A single stage configuration was also used on actual liquid load demonstrating possible liquid disinfection through electroporation. However, due to time constraints a cascaded configuration could not be tested on the liquid loads.

6.1.1 Design Observations and Results

The control signaling scheme needed for H-bridge switching was explained using the Π switching technique, this allows cascading of multiple stages for a multilevel output profile. These signals were produced using a AT90PWM2B MCU, it allowed the output profile to be configurable. Output frequency, frequency of pulses, and number of pulses were configurable parameters available through the MCU interface. The control board was built on a separate PCB board making the pulse generator modular and suitable for other pulse generator designs given similar switching technique. The results showed that the MCU was able to produce accurate timing waveforms for low frequencies of below 100 kHz. At higher frequencies, transitions between switching instructions on the MCU became more visible on the output. Since the MCU clock is limited by the internal oscillator of 16 MHz, a minimum dead-time of 128 ns was therefore used. As shown by the results in Chapter 5, output rise and fall time were significantly smaller than the dead-time; therefore, smaller dead-time could be used to potentially increase dv/dt but also decrease switching losses. While the MCU provided a simple user interface feature and accurate full-bridge signals, the limitations of the MCU meant that the pulse generator could not be tested at higher frequencies (>300 kHz) or various other output profiles. The current MCU board is suitable for disinfection purposes were the output frequency is less than about 300 kHz.

The prototype full-bridge stage using the LM5104 half-bridge driver was built and was useful for a single stage design. However, it was a basic design to see if it could be used in a cascaded configuration. Section 5.2 describes the results achieved. Ringing was observed at high frequencies which was the result of inadequate grounding. PCB layout was not as carefully considered in terms of high -frequency design. Traces tended to be long and thin which can give rise to increased parasitic effects. The output voltage level was limited to 100 V_p, as defined specifications of the internal bootstrap diode of the LM5104. Relatively noise free symmetrical bipolar output results were obtained for a 2 kΩ resistive load. Since the load current is relatively small, high frequency ringing was not as apparent.

HV and LV stages were built and tested for switching voltages of up to 1 kV_p and 400 V_p respectively. The TC4422 MOSFET drivers with ATP7F120B MOSFETs and IXFH14N100Q2 MOSFETs both performed reliably at switching frequencies of below 200 kHz with moderate resistive load of 200 Ω. It was found that the LV board had very fast dv/dt on the output exceeding the MOSFET specifications; this is due to the very low gating resistance. High di/dt of the gate is a result of little gate resistance. Noise on the output was seen to be more apparent. Furthermore, the IXFH14N100Q2 MOSFETs had slightly larger parasitic capacitance giving rise to greater ringing effects. The apparent noise on the gate waveforms did not have a significant effect on output results. The output results for the HV stage performed considerably better, resistive

switching at 2 kV_{pp} had very little noise with fast switching transitions.

A cascaded configuration was successfully demonstrated, no apparent switching noise on the output was seen for a 200 Ω simulated load at frequencies below 100 kHz. Above 100 kHz the limitations of the MCU became more evident. A bipolar staggered wave shape (Figure 5.13) was produced using different voltage levels; this type of waveform is suitable for high frequency biomedical applications. A staggered staircase output profile (Figure 5.14) was successfully produced to meet the specifications of the project and is suitable for disinfection purposes. Output rise dv/dt exceeded 20 V/ns for the HV stage using primarily resistive loads.

Single stage testing was conducted on water and milk which yielded results similar to the resistive loads. Using an electrode apparatus high voltage pulsing was observed across water and milk. The results show that it was consistent with a 200 Ω load. Voltage waveforms for water and milk were similar given an electrode spacing of 1 mm. The measured results were within the limits of the MOSFET specifications.

6.2 FUTURE WORK

There is functionality on the MCU board which is currently not implemented. The MCU code can only produce staircase output waveforms with a fixed HV output pulse width. Modification to the MCU code could provide provisions for various wave-shapes and greater range of output frequencies. There is further scope for the development of a different control board involving the use of an FPGA for pulse signal generation. FPGAs can generate output pulse width frequencies in the order of MHz and therefore could be useful in determining maximum performance of the pulse generator. A dead-time user setting would also be easier to implement. However, development of a FPGA board will involve more complex and unnecessary circuitry compared to the MCU board.

The gate waveforms appeared to show high-frequency noise as well as a possible shoot-through condition; further investigation and testing needs to be undertaken to identify a solution. Naturally, another revision of the pulse generator boards could be built using similar components for higher frequency operation. The modular arrangement of the cascaded topology may introduce potential switching noise on the output. Therefore, a twisted pair in conjunction with a toroid is ideal for minimising coupling of noise between control signal generation and opto-couplers. For high-frequency electroporation applications, loop areas are required to be reduced further. However, using the current cascaded arrangement, no high-frequency switching noise was visible on the output at frequencies below 200 kHz. Of most concern, the inverted output of the opto-isolation section results in a *always on* output. Inadverantly removing any control signals will result in a shoot through condition. Therefore, a simple modification to

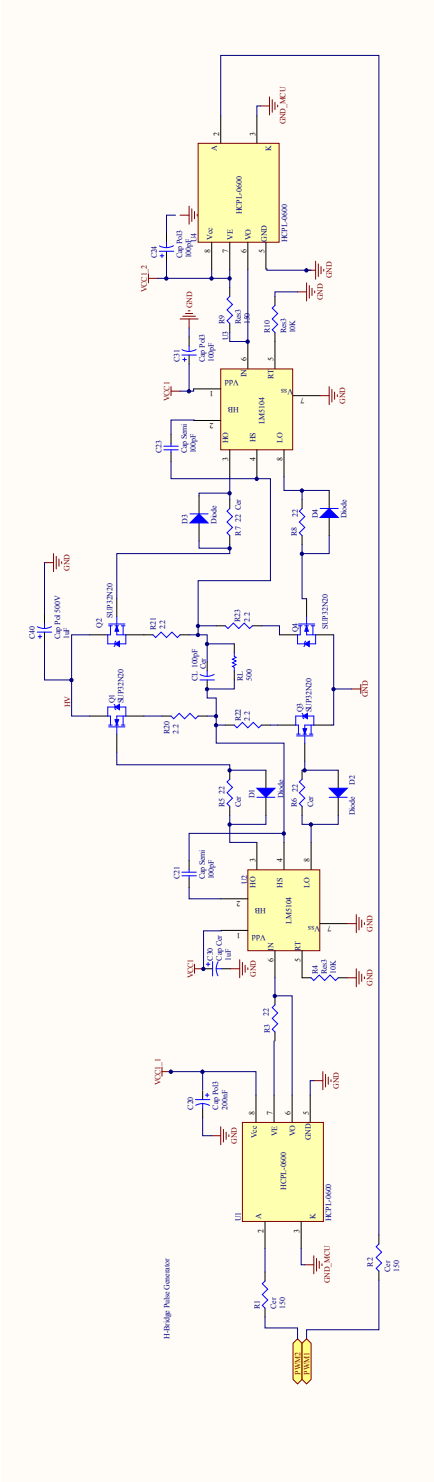
the design and PCB is to use a pull down resistor on the open-collector output, this will result in a non-inverted output.

Lastly, limited tests were performed on actual liquid samples. Further testing of biological or liquid samples is required to see how effective the pulse generator system is in terms of kill rates, and effectiveness at electroporation. The switching effects on the pulse generator using such liquid and biological loads also needs to be investigated.

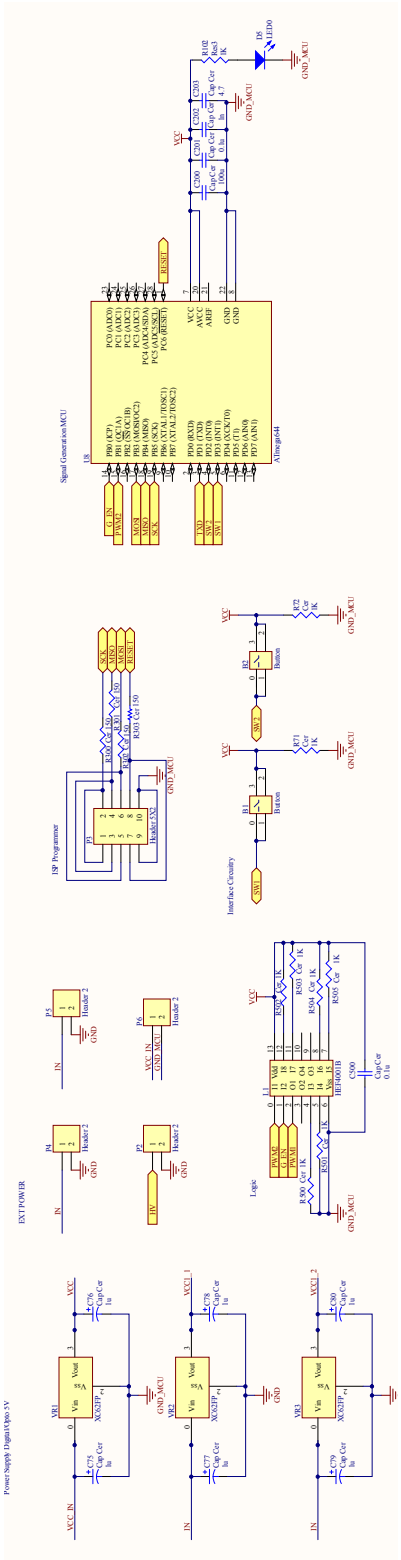
Appendix A

DESIGN SCHEMATICS

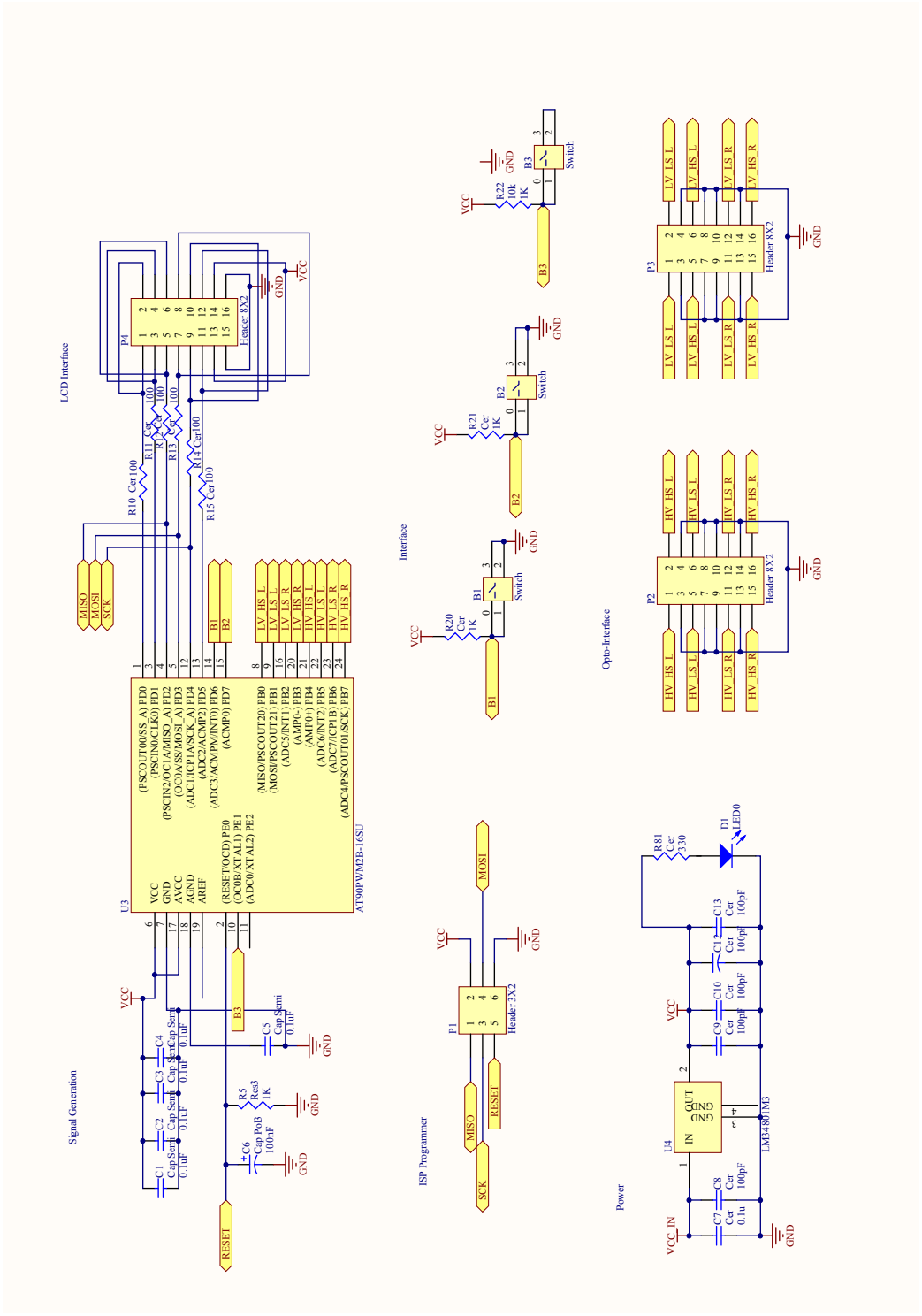
A.1 LOW-VOLTAGE STAGE



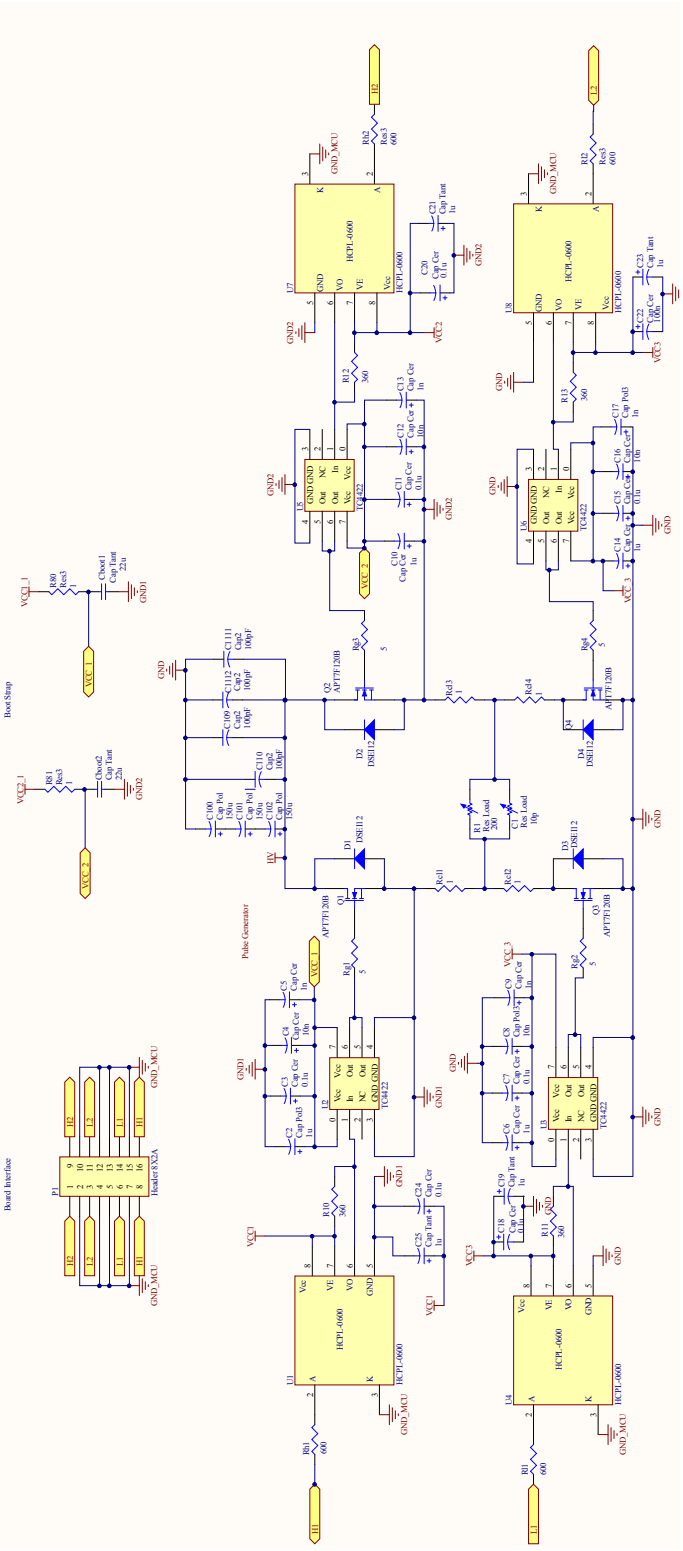
A.2 LOW-VOLTAGE STAGE



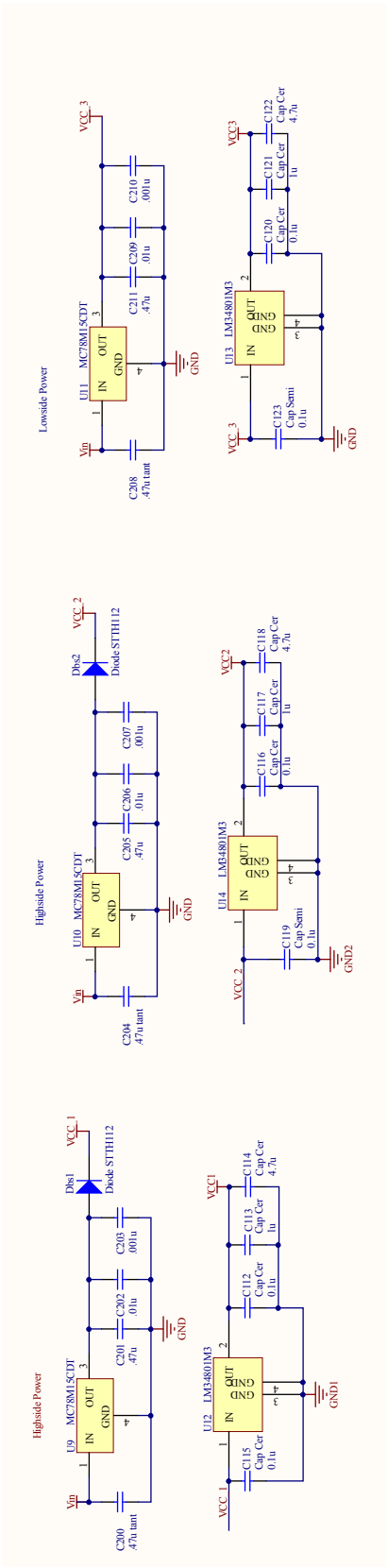
A.3 DIGITAL PULSE SIGNAL GENERATION



A.4 HIGH-VOLTAGE STAGE



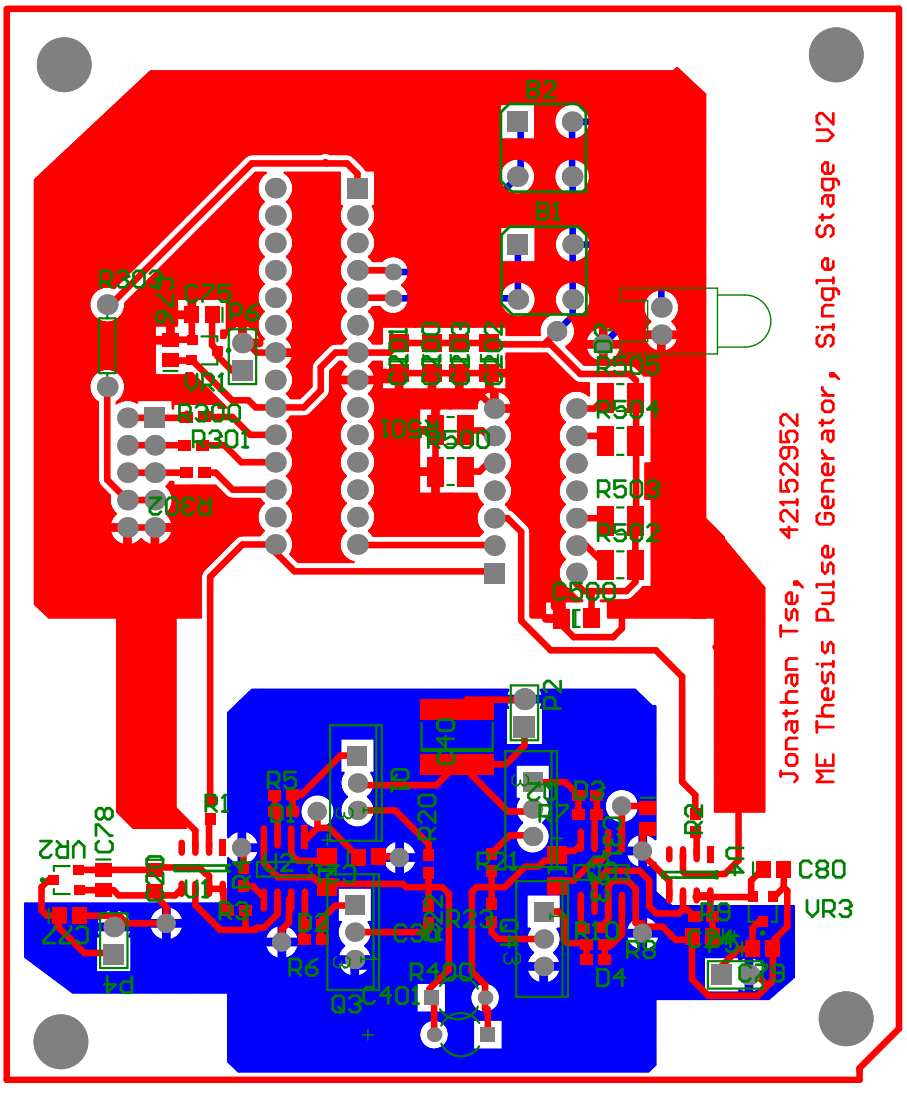
A.5 POWER SUPPLY



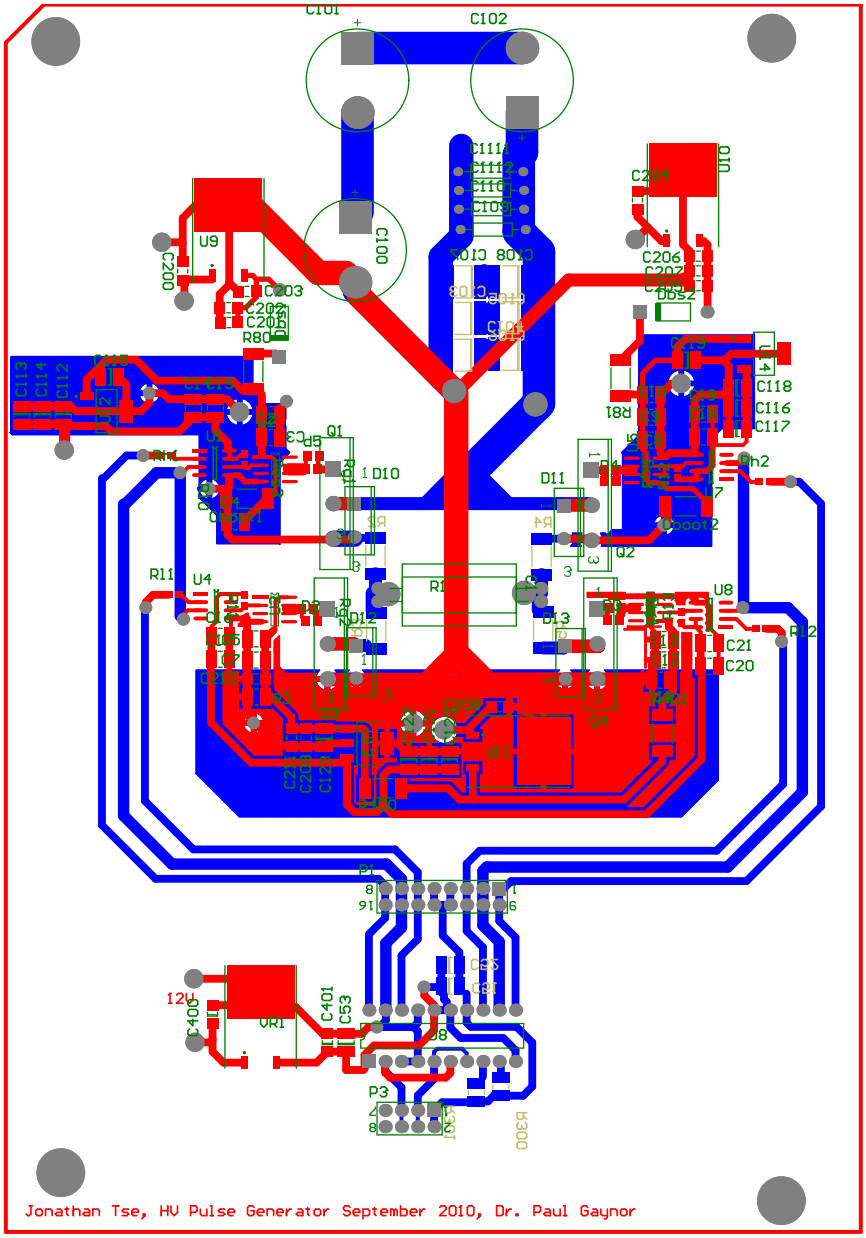
Appendix B

PCB LAYOUT

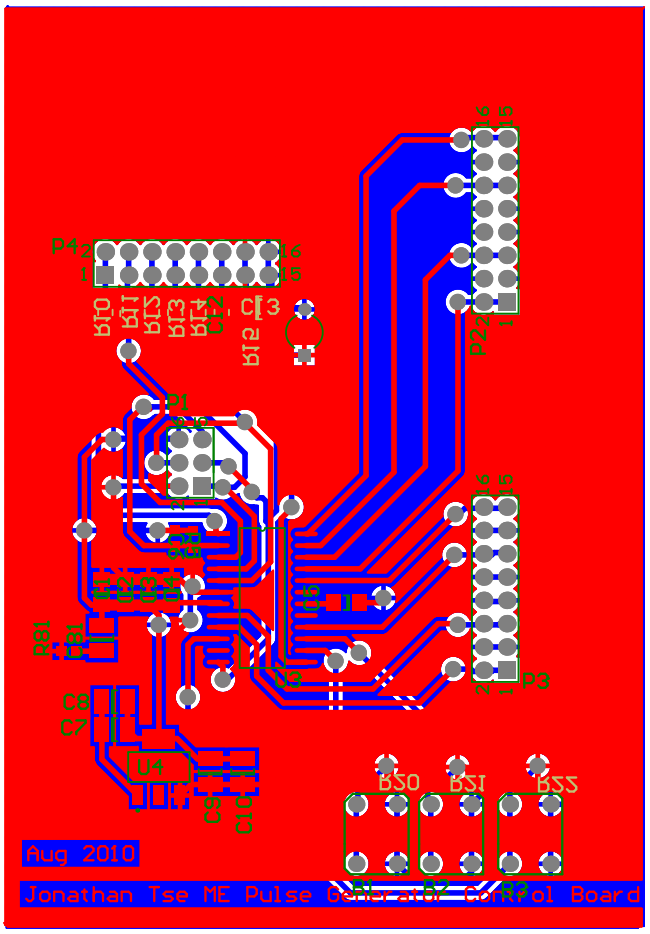
B.1 LOW VOLTAGE STAGE



B.2 HIGH VOLTAGE STAGE



B.3 DIGITAL PULSE GENERATION AND CONTROL



Appendix C

BILL OF MATERIALS / MAJOR COMPONENTS

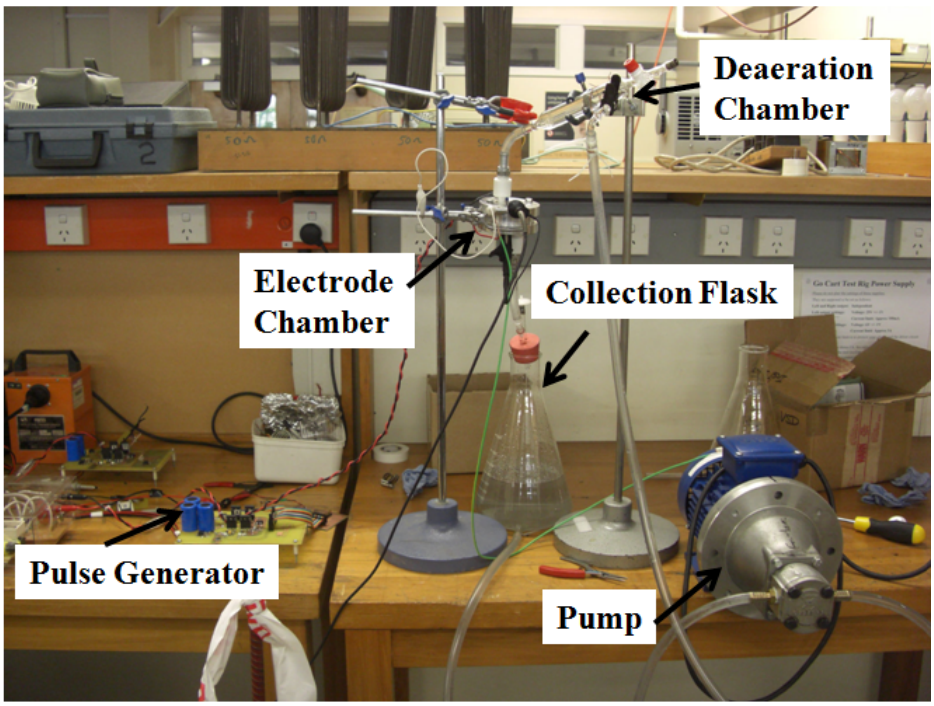
Part Description	Manufacturer	Package	Value	Tolerance	Supplier	#
Low-Voltage Stage						
SUP32N20 MOSFET	Vishay	TO-220	NA	NA	Farnell	4
LM5104 Half-bridge	National Semi	SOIC-8	NA	NA	Farnell	2
HCLP-0601 Opto	Fairchild	SOIC-8	NA	NA	Farnell	2
5V Regulator	Torex	SOT-23	NA	NA	Farnell	2
Resistor	NA	0604	10 kΩ	NA	Farnell	2
Tantalum Capacitor	NA	1206	1.0 uF	5%	Farnell	8
Ceramic Capacitor	NA	1206	1 nF	5%	Farnell	8
Ceramic Capacitor	NA	1206	10 nF	5%	Farnell	8
MCU 8-bit AVR8	Atmel	NA	NA	NA	Farnell	1
High-Voltage Stage						
IXFH14N100Q2 MOSFET	IXYS Coorp	TO-247	NA	NA	Digikey	4
ATP7F120B	Microsemi	TO-247	NA	NA	Digikey	8
TC4422 Driver	Microchip	SOIC-8	NA	NA	Farnell	8
HCLP-0601 Opto	Fairchild	SOIC-8	NA	NA	Farnell	8
1.2kV Diode	IXYS Coorp	TO-220	NA	NA	Farnell	4
Capacitor Electrolytic	Vishay	10mm	150 uF 450V	20%	Farnell	5
Capacitor Ceramic	NA	1206	10 nF 5kV	10%	Farnell	4
Capacitor Ceramic	NA	1206	1 nF 5kV	10%	Farnell	4
Tantalum Capacitor	AVX	2917	22uF 35V	10%	Farnell	4
Thickfilm Resistor	Tyco	NA	200 Ω 10 W	5%	Farnell	2
Resistor 2W	Yageo	2512	1 Ω	5%	Farnell	8
Tantalum Capacitor	NA	1206	1.0 uF	5%	Farnell	8
Ceramic Capacitor	NA	1206	1 nF	5%	Farnell	8
Ceramic Capacitor	NA	1206	10 nF	5%	Farnell	8
Ceramic Capacitor	NA	1206	0.1 uF	5%	Farnell	8
Resistor	NA	0604	150 Ω	10%	Farnell	8
16 pin Socket	NA	2.54mm	NA	NA	Farnell	4
15V Regulator 1.5A	STMICROELECTRONICS	D2PAK	NA	NA	Farnell	6
5V Regulator	National Semi	SOT-223	NA	NA	Farnell	6
Fast Blow fuse	NA	NA	4A	NA	Farnell	2

Part Description	**Manufacturer**	**Package**	**Value**	**Tolerance**	**Supplier**	#
Digital Control Board						
AVRPWM2B MCU	Atmel	NA	NA	NA	Farnell	1
5V Regulator	National Semi	SOT-223	NA	NA	Farnell	6
Tatile button	NA	NA	NA	NA	Farnell	3
16 Header	NA	2.54	NA	NA	Farnell	2
LCD 16x2	Sitronix	NA	NA	Na	Farnell	1

Appendix D

ELECTRODE SYSTEM FOR DISINFECTION APPLICATIONS

The electrode chamber for liquid disinfection was designed and built by Jonathan Bousfield at the University of Canterbury. Mr Bousfield was working a similar project involving liquid disinfection through electroporation. The electrode apparatus consisted of a stainless steel 1 mm × 1mm electrode arrangement. Variable spacing between positive and negative electrodes was possible. A simple pump was used to push liquid through the electrode system at a constant rate. He also used a deaeration chamber to remove trapped air bubbles as to prevent arching between electrodes which could damage the pulse generator. For the initial testing of the pulse generator, a 1 mm electrode gap was used in order to understand the how a liquid load will effect the pulse generator.



Appendix E

SOFTWARE CODE FOR AT90PWM2B

```
#define F_CPU 16000000UL

//
//Modified 16/9/11
//Name: Jonathan Tse B.E. (Hons)
//Cascaded HV Pulse Generator, Univerity of Canterbury, New Zealand
//

#include <avr/io.h>
#include <stdint.h>
#include <stdlib.h>
#include <util/delay.h>
#include <avr/eeprom.h>

#include "lcd_functions.h"
#include "pulser.h"

//
//initalise timer1
//RETURN: NULL
void init_timer1(void) {
  //64 prescale on 16 Mhz clock
  TCCR1B |= (1<<CS12)|(1<<CS10);
}

//
//initalise timer0
//RETURN:   NULL
void init_timer0(void) {
  TCCR0B |= (1<<CS02)|(1<<CS00);
}

//
//initalise I/O Pins
//RETURN:   NULL
void init_gpio(void) {
  //Set outputs for H-Bridge Pins
  DDRB |= (1<<PIN7)|(1<<PIN6)|(1<<PIN5)|(1<<PIN4)|(1<<PIN3)|(1<<PIN2)|(1<<PIN1↩
      )|(1<<PIN0);  //set as outputs
  PORTB = 0x00; //all outputs
  HV_HS_R_H();  //initially set for bootstrap capacitors
  HV_HS_L_H();
  LV_HS_L_H();
  LV_HS_R_H();
}

//
//button check fuction
```

```
//PARAMETERS:    Button number
//RETURN:      0 = no button, else button number
unsigned int button_check(unsigned int i) {
  switch(i) {
    case 1:
      if(BUTTON1) {
        _delay_ms(20);
        while(BUTTON1) {;}
        return 1;
      }
      else {
        return 0;
      }
    case 2:
      if(BUTTON2) {
        _delay_ms(20);
        while(BUTTON2) {;}
        return 1;
      }
      else {
        return 0;
      }
    case 3:
      if(BUTTON3) {
        _delay_ms(20);
        while(BUTTON3) {;}
        return 1;
      }
      else {
        return 0;
      }
      default:
        return 0;
      }
}

//
//pulse width output function
//PARAMETERS: int frequency as defined by table in pulser.h
//        int pulses, number of pulses
//        uint16_t delaytime, delay period between pulse train
//
//RETURN:   NULL
void pulse_output(unsigned int frequency, unsigned int pulses, uint16_t ↩
    delaytime) {
  update_temp exit = false;

  int i,j = 0;
    while(!exit) {
      //timer delay
      if( delaytime != 0) {
        TCNT1 = 0;
        while(TCNT1 < delaytime) {
        ;
        }
      }

      for(i=0;i<pulses;i++) {



        //Low-voltage stage first
        LV_LS_L_H(); //low
        LV_HS_L_L(); //high

        LV_HS_R_H();
        LV_LS_R_L();
```

```
        //High-voltage stage second
        HV_LS_L_H();
        HV_HS_L_L(); //left HS high



        for(j=0;j<frequency;j++)
        {
          asm volatile ("nop");
        }

        //High-voltage stage
        HV_LS_R_H();
        HV_HS_R_L(); //right LS low

        for(j=0;j<frequency;j++)
        {
          asm volatile ("nop");
        }



        //Low-voltage stage first
        LV_HS_L_H();
        LV_LS_L_L();
        LV_LS_R_H();
        LV_HS_R_L();

        //High-Voltage stage second
        HV_HS_L_H();
        HV_LS_L_L();


          for(j=0;j<frequency;j++)
        {
          asm volatile ("nop");
        }

        //High-voltage
        HV_HS_R_H();
        HV_LS_R_L();

        for(j=0;j<frequency;j++)
        {
          asm volatile ("nop");
        }



      }
      //Low-side Reset Boot-strap
      LV_HS_R_H();
      LV_LS_R_L();

      if(button_check(ENTER)) {
        exit = true;
        break;
      }
    }
}

//functions for EEPROM (NOT yet implemented)
void read_setup(void) {
  ;
}
//functions for EEPROM (NOT yet implemented)
void write_setup(void) {
  ;
```

```
}


//main control board routine
int main(void) {

  unsigned int pulses_t = PULSES;      //default number of pulses in the pulse ↩
      train
  unsigned int frequency_t = DEF_FREQ;  //default frequency setting
  unsigned int delay = 7;          //default delay setting

  enum menu current = run;
  update_temp update = true;


  init_gpio();
  init_timer1();



  lcd_init();
  lcd_comm_wr(CLEAR);
  lcd_locate_cursor(0);
  _delay_ms(1000);
  lcd_pstring("High Voltage");
  lcd_locate_cursor(LINE2);
  lcd_pstring("Pulse Generator");
  _delay_ms(2500);

  lcd_clear();
  lcd_home();
  lcd_pstring("Loading setup");
  lcd_cursor_on();

  _delay_ms(2500);
  lcd_cursor_off();


  while(1) {

      //Check Button presses
      if(button_check(NEXT)) {
        current++;
        if(current >= menu_items) {
          current=0;
          }

        update = true;
      }
      if(button_check(BACK)) {
        if(current == 0) {
          current=menu_items-1;
        } else {
          current--;
        }
        update = true;
      }



      switch(current) {
        //RUN PULSER
        case run:
          if(update) {
            lcd_clear();
            lcd_home();
            lcd_pstring("Run pulser...");
            lcd_locate_cursor(14);
            lcd_data_wr(LEFT_ARROW);
```

```
      lcd_locate_cursor(15);
      lcd_data_wr(RIGHT_ARROW);
      update = false;
    }
    if(button_check(ENTER)) {
      lcd_clear();
      lcd_home();
      lcd_line2();
      lcd_cursor_on();
      lcd_pstring("Running");
      pulse_output(table[frequency_t][1], pulses_t, delay_table[delay↩
          ][1]);

      lcd_cursor_off();
      update = true;

    }
    break;

  //MODIFY PULSES
  case pulse:
    if(update) {
      lcd_clear();
      lcd_home();
      lcd_pstring("Pulses...");
      lcd_locate_cursor(14);
      lcd_data_wr(LEFT_ARROW);
      lcd_locate_cursor(15);
      lcd_data_wr(RIGHT_ARROW);
      update = false;
    }
    if(button_check(ENTER)) {
      char buff[16];
      lcd_clear();
      lcd_home();
      lcd_pstring("Pulses?");
      update = true;

      while(1) {

        if(button_check(NEXT)) {
          if(pulses_t < 200) {
            pulses_t++;
            update = true;
          }

        }

        if(button_check(BACK)) {
          if(pulses_t > 2) {
            pulses_t--;
            update = true;
          }
        }

        if(button_check(ENTER)) {
          update = true;
          lcd_cursor_off();
          lcd_clear();
          lcd_home();
          lcd_pstring("Set!");
          _delay_ms(1000);
          break;
        }

        if(update) {
          itoa(pulses_t, buff, 10);
          lcd_clear();
          lcd_home();
```

```
            lcd_pstring("Pulses?");
            lcd_line2();
            lcd_pstring(buff);
            lcd_cursor_on();
            update = false;
          }
        }

      }
    break;
    //MODIFY ONTIME FOR LOW-VOLTAGE STAGE
    case frequency:
      if(update) {
        lcd_clear();
        lcd_home();
        lcd_pstring("Frequency...");
        lcd_locate_cursor(14);
        lcd_data_wr(LEFT_ARROW);
        lcd_locate_cursor(15);
        lcd_data_wr(RIGHT_ARROW);

        update = false;
      }
      if(button_check(ENTER)) {
        char buff[16];
        lcd_clear();
        lcd_home();
        lcd_pstring("Frequency?");
        update = true;

        while(1) {
          if(button_check(NEXT)) {
            if(frequency_t < LV_FREQ-1) {
              frequency_t++;
              update = true;
            }

          }

          if(button_check(BACK)) {
            if(frequency_t > 0) {
              frequency_t--;
              update = true;
            }
          }

          if(button_check(ENTER)) {
            update = true;
            lcd_cursor_off();
            lcd_clear();
            lcd_home();
            lcd_pstring("Set!");
            _delay_ms(1000);
            break;
          }

          if(update) {
                itoa(table[frequency_t][0], buff, 10);
                lcd_clear();
                lcd_home();
                lcd_pstring("Frequency?");
                lcd_line2();
                lcd_pstring(buff);
                lcd_locate_cursor(20);
                lcd_pstring("kHz");
                lcd_cursor_on();
                update = false;
          }
        }
```

```
    }
    break;

  //MODIFY DELAYTIME
  case delaytime:
    if(update) {
      lcd_clear();
      lcd_home();
      lcd_pstring("Delaytime...");
      lcd_locate_cursor(14);
      lcd_data_wr(LEFT_ARROW);
      lcd_locate_cursor(15);
      lcd_data_wr(RIGHT_ARROW);

      update = false;
    }
    if(button_check(ENTER)) {
      char buff[16];
      lcd_clear();
      lcd_home();
      lcd_pstring("Delaytime?");
      update = true;

      while(1) {
        if(button_check(NEXT)) {
          if(delay < DELAYS-1) {
            delay++;
            update = true;
          }

        }

        if(button_check(BACK)) {
          if(delay > 0) {
            delay--;
            update = true;
          }
        }

        if(button_check(ENTER)) {
          update = true;
          lcd_cursor_off();
          lcd_clear();
          lcd_home();
          lcd_pstring("Set!");
          _delay_ms(1000);
          break;
        }

        if(update) {
              itoa(delay_table[delay][0], buff, 10);
              lcd_clear();
              lcd_home();
              lcd_pstring("Delaytime?");
              lcd_line2();
              lcd_pstring(buff);
              lcd_locate_cursor(21);
              if(delay_table[delay][2] == 0) {
                lcd_pstring("uS");
              } else {
                lcd_pstring("mS");
              }
              lcd_cursor_on();
              update = false;
        }
      }
    }
    break;
    case save:
```

```
            if(update) {
              lcd_clear();
              lcd_home();
              lcd_pstring("Save...");
              lcd_locate_cursor(14);
              lcd_data_wr(LEFT_ARROW);
              lcd_locate_cursor(15);
              lcd_data_wr(RIGHT_ARROW);

              update = false;
            }
            if(button_check(ENTER)) {
              lcd_clear();
              lcd_home();
              lcd_pstring("Save?");
              update = true;

            }
          break;
        default:
          break;
      }
  }

}



#define F_CPU 16000000UL

//Modified 9/12/10
//Name: Jonathan Tse
//ME Pulse Generator, Univerity of Canterbury, New Zealand

//Header File pulser.h

#include <avr/io.h>
#include <stdint.h>
#include <stdlib.h>
#include <util/delay.h>
#include <avr/eeprom.h>
#include "lcd_functions.h"

#define LV_FREQ 6
#define DELAYS 8

//Default Settings
#define DEF_FREQ 3
#define DELAY 100

//EEPROM Memory Addresses
#define F_ADDR 1
#define P_ADDR 2
#define D_ADDR 3

//Frequency setting table
static uint16_t table[LV_FREQ][2] = {
{250, 0},
{200, 1},
{100, 3},
{50, 9},
{10, 60},
{1, 580}
};

//Delay time settings table
/*static uint16_t delay_table[DELAYS][2] = {
{0, 0 },
{50, 13},
```

```
{100, 25},
{200, 50},
{500, 125},
{1000, 300},
{2000, 600},
{5000, 1250},


};*/

static uint16_t delay_table[DELAYS][3] = {
{0, 0, 0 }, //us
{64, 1, 0},
{128, 2, 0},
{512, 8, 0},
{1, 16, 1}, //ms
{64,1000, 1},
{128, 2000,1},
{512, 8000,1},


};



//Menu configrations
enum menu {run = 0, frequency, pulse, delaytime, save};
static int menu_items = 5;
enum bool {false=0, true};
typedef int update_temp;

//High voltage stage
//Port B PINS 4-7
//right H-bridge
#define HV_HS_R_H() PORTB |= (1<<PIN7)
#define HV_HS_R_L() PORTB &= ~(1<<PIN7)
#define HV_LS_R_H() PORTB |= (1<<PIN6)
#define HV_LS_R_L() PORTB &= ~(1<<PIN6)
//left H-bridge
#define HV_LS_L_H() PORTB |= (1<<PIN5)
#define HV_LS_L_L() PORTB &= ~(1<<PIN5)
#define HV_HS_L_H() PORTB |= (1<<PIN4)
#define HV_HS_L_L() PORTB &= ~(1<<PIN4)

//Low Voltage stage
//Port B PINs 0-3
//right H-bridge
#define LV_HS_R_H() PORTB |= (1<<PIN3)
#define LV_HS_R_L() PORTB &= ~(1<<PIN3)
#define LV_LS_R_H() PORTB |= (1<<PIN2)
#define LV_LS_R_L() PORTB &= ~(1<<PIN2)
//left H-bridge
#define LV_LS_L_H() PORTB |= (1<<PIN0)
#define LV_LS_L_L() PORTB &= ~(1<<PIN0)
#define LV_HS_L_H() PORTB |= (1<<PIN1)
#define LV_HS_L_L() PORTB &= ~(1<<PIN1)

//Default configuration
#define PULSES 10
#define FREQUENCY 3

//Button configration
#define BUTTON2 ~PIND & (1<<6)
#define BUTTON1 ~PINE & (1<<1)
#define BUTTON3 ~PIND & (1<<7)
#define ENTER 2
#define NEXT 1
#define BACK 3
```

```
//Prototype fucuntions
void init_timer1(void);

void init_timer2(void);

void init_gpio(void);

unsigned int button_check(unsigned int i);

void pulse_output(unsigned int frequency, unsigned int pulses, uint16_t ↩
    delaytime);
```

REFERENCES

Alexander, S.A. (2009), 'Digital switching scheme for cascaded multilevel inverters', *Third International Conference on Power Systems*.

Alkhafaji, S.R. and Farid, M. (2007), 'An investigation on pulsed electric fields technology using new treatment chamber design', *Innovative Food Science and Emerging Technologies*, Vol. 8, pp. 205–212.

Ardizzoni, J. (2005), 'A practical guide to high-speed printed-circuit-board layout', *Analog Dialogue*.

Atlas, R.M. (1988), *Microbiology Fundamentals and Applications*, MacMillan Publishing, United States of America.

ATmel Cooperation (2006), 'AT90PWM2B', datasheet.

Atmel Corporation (2010), 'Avr hardware design considerations', Design Notes. Application Note AVR042.

Baek, J., Ryu, M., Yoo, D. and Kim, H. (2002), 'High voltage pulse generator using boost array converter', *Industrial Electronics Society, IEEE, 28th*, Vol. 1, pp. 395 – 399.

Ball, A. (2005), *Thermal Stability of MOSFETs AND8199*, Technical Report, On Semiconductor.

Balogh, L. (2001), *Design and Application Guide For High Speed MOSFET Gate Drive Circuits*, Technical Report, Texas Instruments.

Barkhordarian, V. (2005), *Power MOSFET Basics*, Technical Report, International Rectifier.

Bildgen, M. (2004), *Resonant Converter Topologies*, Technical Report, ST Microelectronics.

BTX (2011), 'Square wave electroporator', Website, January. `http://www.btxonline.com/products/electroporation/Default.asp`.

Castro, A., Barbosa-Canovas, G. and Swanson, B. (1993), 'Microbial inactivation of foods by pulsed electric fields', *Journal of Food Processing and Preservation*, Vol. 17, pp. 47–73.

Chaney, A. and Sundararajan, R. (2004), 'Simple mosfet-based high-voltage nanosecond pulsed circuit', *IEEE Transactions on Plasma science*, Vol. 32, No. 5, pp. 1919–1924.

Chen, G. (2005), *High Voltage Pulse Generator Design for Electroporation Research*, Master's thesis, The University of Waikato.

Chen, L. and Peng, F.Z. (2008), 'Dead-time elimination for voltage source inverters', *IEEE Transactions on Power Electronics*, Vol. 23, No. 2.

Chen, C., Evans, J., Robinston, M., Smye, S. and Toole, P. (2008), 'Measurement of the efficiency of cell membrane electroporation using pulsed ac fields', *Physics in Medicine and Biology*, No. 53, pp. 4747–4757.

Corzine, K. and Familiant, Y. (2002), 'A new cascaded multilevel h-bridge drive', *IEEE Transactions on Power Electronics*, Vol. 17, No. 1, pp. 125–131.

Dodge, J. (2004), *Eliminating Parasitic Oscillation between Parallel MOSFETs*, Technical Report, Advanced Power Technology.

Dunn, J. (2004), *Matching MOSFET Drivers to MOSFETs AN7899*, Technical Report, Microchip Tehcnology Inc.

Elbanhawy, A. (2008), *Effect of Source Inductance on MOSFET Rise and Fall Times*, Technical Report, Maple Soft.

Fairchild Semiconductor (2008), 'Design and application guide of a bootstrap circuit for high-voltage gate-drive ic', Application note.

Grenier, J.R. and Kazerani, M. (2008), 'Mosfet-based pulse power supply for bacterial transformation', *IEEE Transactions on Industry Applications*, Vol. 44, No. 1, pp. 25–31.

Hanifah, J., Azli, N.A., Afendi, M. and Piah, M. (2010), 'Cascaded h-bridge multilevel inverted based pulsed power supply for liquid food sterilization'.

Hart, D.W. (1997), *Introduction to Power Electronics*, Prentice Hall, Upper Saddle River, NJ.

Hewlett Packard (2007), 'Common-mode noise: Sources and solutions'. Application note AN1043.

Information Unlimited (2011), 'CHARGE5000 PSU', Website. http://www.amazing1.com/hv-dc-power-supplies.htm.

International Rectifier (2007), 'HV Floating MOS-Gate Driver ICs', Application note.

Jayaram, S.H., El-Hag, A.H., Espino-Cortex, F.P., Wong, R. and Leibovitch, C. (2005), 'Effects of process and product parameters of the nanosecond pulses used in high-field liquid food treatment', *IEEE Transactions on Industry Applications*, Vol. 41, No. 2, pp. 520–526.

Johnstone, P.T. (2001), *Applications of High Voltage Power Supplies in the Purification of Water*, PhD thesis, University of Canterbury, Christchurch, New Zealand.

Joshi, M. and Argarwal, V. (1999), 'Component placement for improved emi performance in power electronic circuits', *Applied Power Electronics Conference and Exposition*, Vol. 2, pp. 911–917.

Kang, F., Park, S., Kim, C. and Cho, S.E. (2004), 'Half-bridge and full-bridge cell base multilevel pwm inverter with cascaded transformers', *The 47th IEEE international Midwest Symposium on Circuits and Systems*, Vol. 2.

Karunakaran, S. (2003), 'Techniques to minimise cross-talk and ringing in printed circuit boards', *Electromagnetic Interference and Compatibility*, pp. 65–68.

Katrai, C. and Arcus, C. (1998), *EMI Reduction Techniques*, Technical Report, Pericom Semiconductor Corporation.

Koonce, D. (2003), *Integrating MOSFETs and Drive Circuitry For Power Supply Applications*, Technical Report, Vishay Siliconix, Santa Clara, CA.

Locher, R. (1988), *Introduction to Power MOSFETs and Their Applications*, Technical Report, National Semiconductor.

Meloncelli, G.P. (2001), *L638X Tricks and Tips*, Technical Report, STMicroelectronics.

Merello, A., Rugginenti, A. and Grasso, M. (2005), *Using Monolithic High Voltage Gate Drivers DT 04-4*, Technical Report, International Rectifier.

Microchip (2005), 'TC4421A/TC4422A 9A High-Speed MOSFET Drivers'. datasheet.

Microsemi Corporation (2011), 'Mosfets', Website. http://www.microsemi.com/.

Mohan, N., Undeland, T. and Robbins, W. (2003), *Power Electronics Converters, Applications and Design*, John Wiley and Sons Inc, 111 River Street, Hoboken, NJ, United State of America.

Oh, K. (2000), *MOSFET Basics*, Technical Report, Fairchild Semiconductor Inc.

Oka, Y., Muramotol, Y., Shimizul, N. and Tchihara, S. (2009), 'Sterilization of liquids by high electric field pulse', *Annual Report Conference on Electrical Insulation and Dielectric Phenomena*.

ON Semiconductor (2006), 'Thyristor theory and design conderations', Application note.

Pavselj, N. and Miklavcic, D. (2008), 'Numerical modeling in electroporation-based biomedical applications', *Radiol Oncol*, Vol. 43, No. 3, pp. 159–168.

Puc, M., Corvic, S., Flisar, K., Petkovsek, M., Nastran, J. and Miklavcic, D. (2004), 'Techniques of signal generation required for electropermeabilization. survey of electropermeabilization devices', *Science direct Biochemistry*, Vol. 64, pp. 113–124.

Rae, J.L. and Levis, R.A. (2002), 'Single-cell electroporation', *European Journal of Physiology*, Vol. 443, No. 4, pp. 664–670.

Randall, R. (2005), *Choosing Power Switching Devices for SMPS Designs*, Technical Report, Fairchild Semiconductor.

Rao, S. (2008), *Sterilization and Disinfection*, Technical Report, Dept. of Microbiology, JJMMC, Davangere.

Rashid, M.H. (2001), *Power Electronics Handbook*, Academic Press, California USA.

Rashid, M.H. (2003), *Power Electronics: Circuit, Devices and Applications. Third Edition*, Pearson, Prentice Hall, Upper Saddle River, NJ 07458.

Ritchey, L.W. (1999), 'A survey and tutorial of dielectric materials used in the manufacture of printed circuit boards.', *Circuittree November Edition*.

Roche, S. (2004), *Solid State Pulsed Power System*, Technical Report, Physique and Industrie.

Rubinsky, B. (2007), 'Irreversible electroporation in medicine', *Technology in Cancer Research and Treatment, Volume 6, Number 4*.

Sattar, A. (1998), *Insulated Gate Bipolar Transistors (IGBT) Basics*, Technical Report, IXYS Corporation.

Schmitz, T. and Wong, M. (2007), *Choosing and Using Bypass Capacitors*, Technical Report, Intersil.

Schoenbach, K.H., Peterkin, F.E., Alden, R.W. and Beebe, S.J. (1997), 'The effect of pulse electric fields on biological cells: Experiments and applications', *IEEE Transactions of Plasma Science, Vol 25, No 2.*

Scoggins, P. (2007), 'A guide to designing gate-drive transformers', *Power Electronics Technology*, pp. 32–36.

Semtech (2004), *High Speed Synchronous Power MOSFET Driver*, Technical Report, Sentech Corporation.

Shen, Z.J., Xiong, Y., Cheng, X., Fu, Y. and Kumar, P. (2006), 'Power mosfet switching loss analysis: A new insight', *Industry Applications Conference, 2006, 41st ISA Annual Meeting.*

Teissie, J., Eynard, N., Vernhes, M., Ganeva, A., Galutzov, B. and Cabanes, P. (2002), 'Recent biotechnological developments in electropulsation. a prospective review', *Bioelectrochemistry*, Vol. 55, No. 1-2, pp. 107–112.

Wetz, D., Truman, K., Dickens, J., Mankowski, J. and Neuber, A. (2004), 'Short pulse electric field sterilization of liquid media', *Centre for Pulsed Power and Power Electronics.*

White, J. (2008), *MOSFET Body Diode*, Technical Report, Hephaestus Audio.

Wu, B. (2006), *High-Power Converters and AC Drives*, John Wiley & Sons Inc, Hoboken, New Jersey.

Young, S. (2004), *Power MOSFET avalanche guideline*, Technical Report, Fairchild Semiconductor Inc.